

# Fonseca 14 UMA Schematics Document

## rPGA988A Mobile Arrandale

### Intel IbeX Peak-M

2010-03-19

[www.aitech1.ru](http://www.aitech1.ru)

REV : -1

*DY : Nopop Component*  
*B\_TPM:Use Lom TPM*  
*C\_TPM:Use China TPM*

<Core Design>

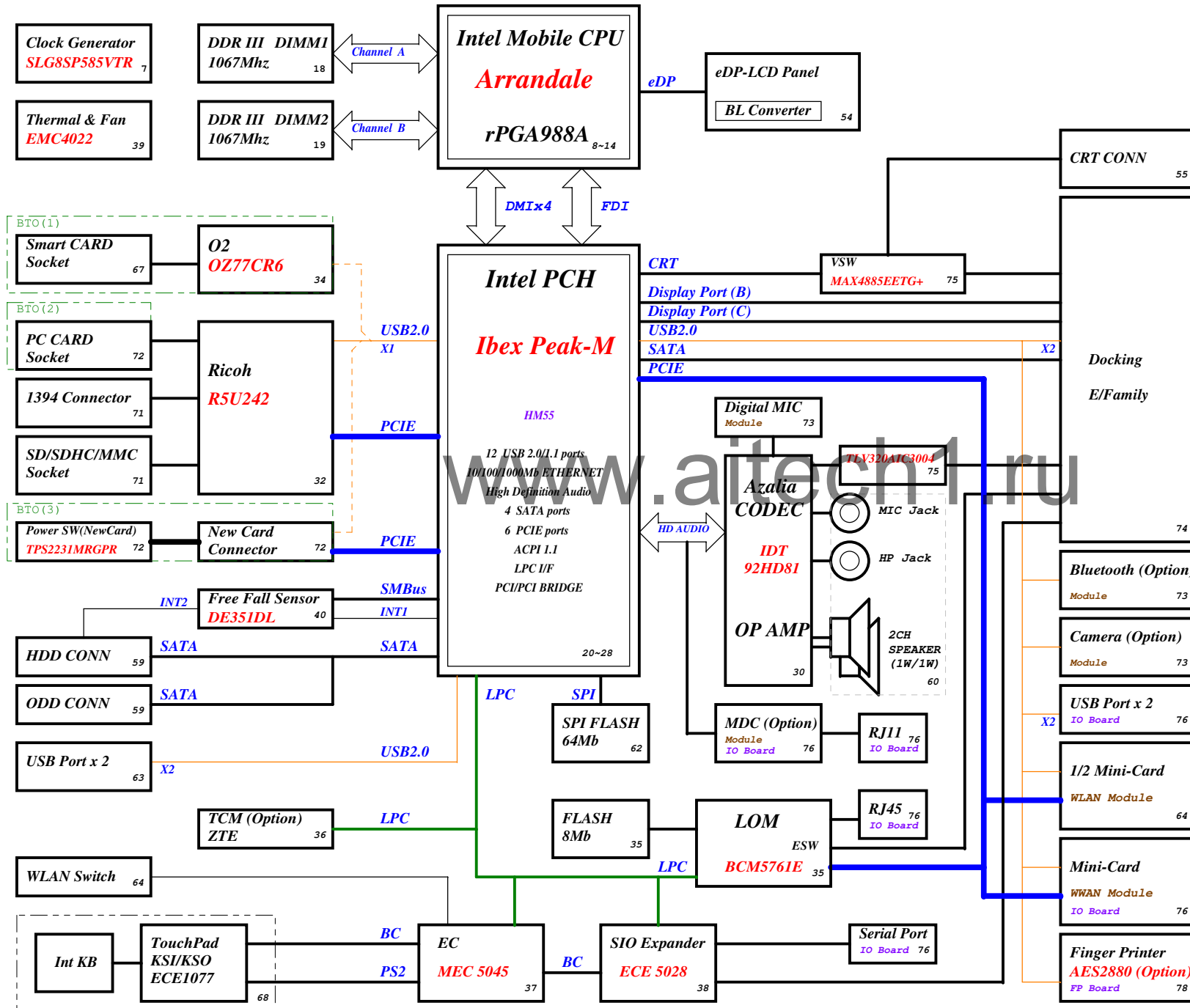


**Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title			<b>Cover Page</b>	
Size	Document Number	Rev		
Custom	<b>Fonseca UMA</b>	<b>X02</b>		
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# Fonseca 14" UMA Block Diagram

	DF3-14
Project code	91.4GN01.001
PCB P/N	48.4GN01.0SC
Revision	09276 - SC



CPU DC/DC ISL62883	
INPUTS	OUTPUTS
+PWR_SRC	+VCC_CORE

SYSTEM DC/DC TPS51125	
INPUTS	OUTPUTS
+PWR_SRC	+3.3V_ALW +5V_ALW

SYSTEM DC/DC TPS51116	
INPUTS	OUTPUTS
+PWR_SRC	+1.5V_SUS +0.75V_DDR_VTT

SYSTEM DC/DC TPS51218	
INPUTS	OUTPUTS
+PWR_SRC	+1.05V_VTT

SYSTEM LDO RT9035	
INPUTS	OUTPUTS
+3.3V_SUS	+1.8V_RUN

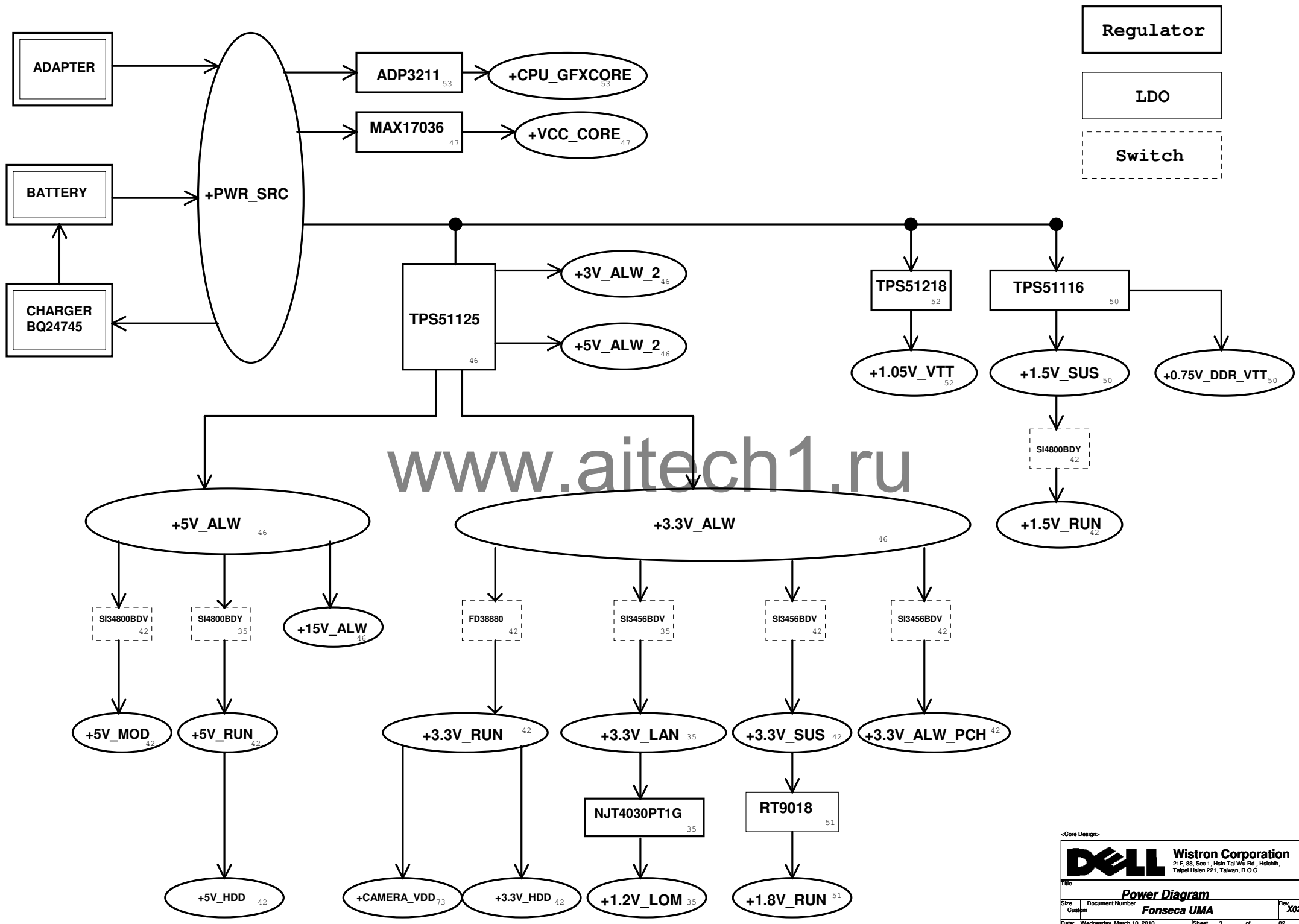
SYSTEM DC/DC ADP3211	
INPUTS	OUTPUTS
+PWR_SRC	+CPU_GFXCORE

BATTERY CHARGER TI BQ24745 (AC, Battery Existence)	
INPUTS	OUTPUTS
+DC_IN_SS	+PBATT

<Core Design>

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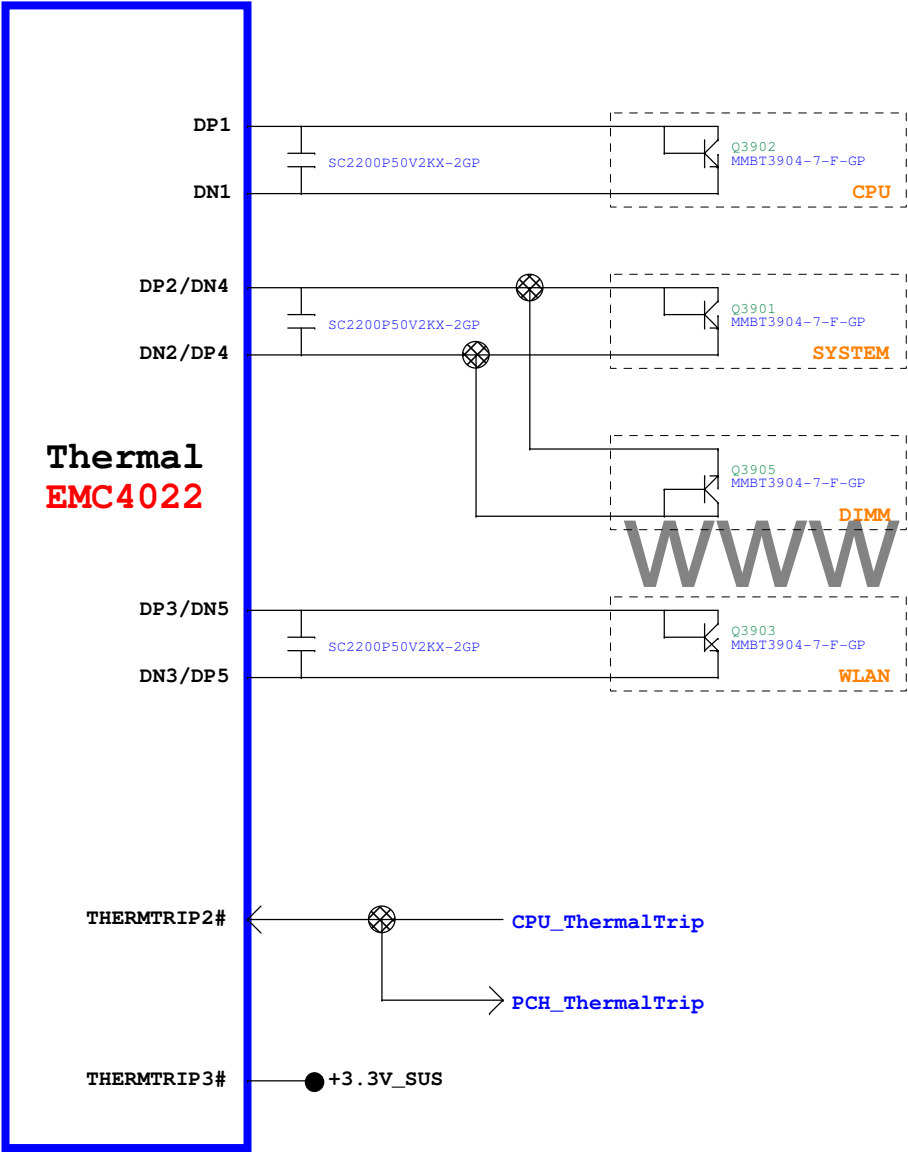
Title: **Block Diagram**  
Size: Custom  
Document Number: **Fonseca UMA**  
Date: Wednesday, March 10, 2010  
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Rev: X02



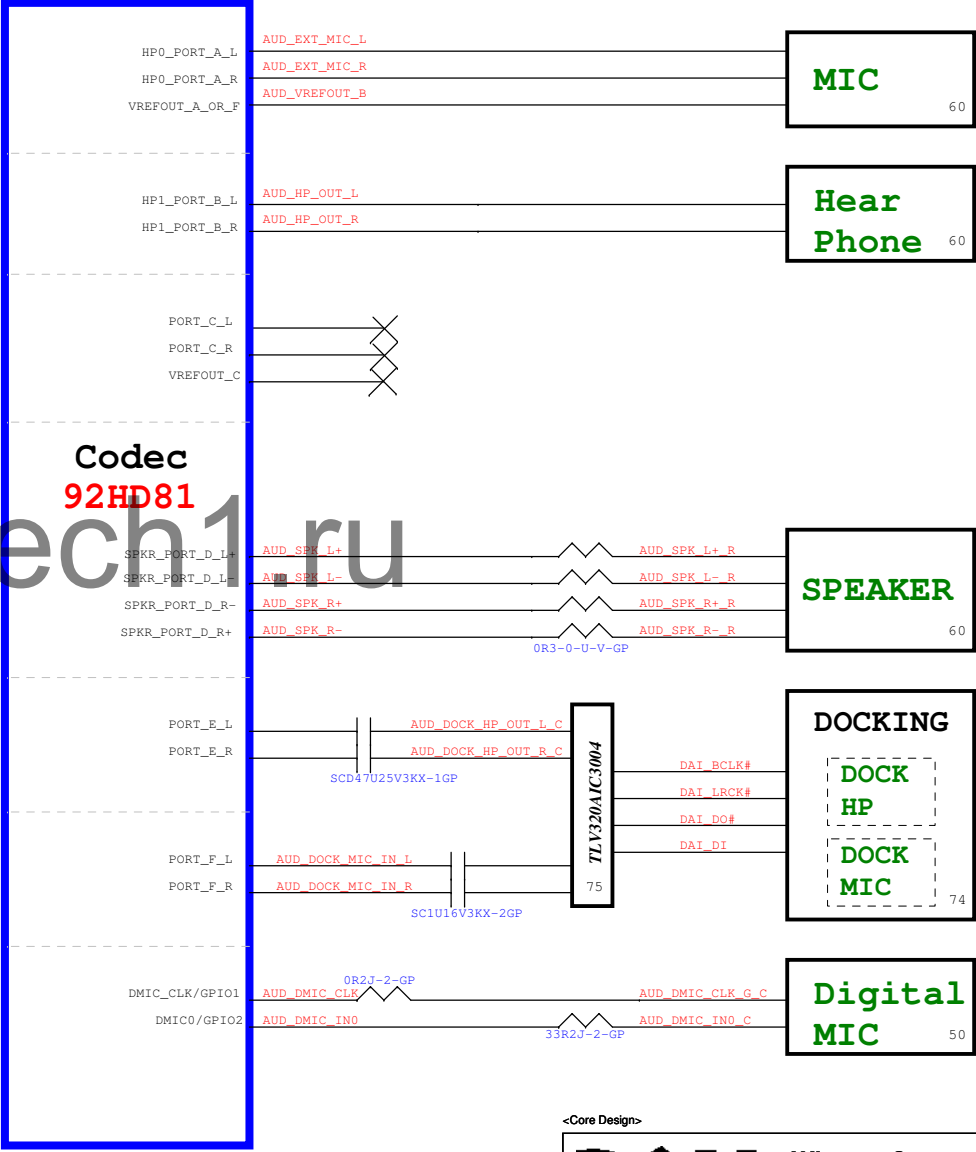




# Thermal Block Diagram



# Audio Block Diagram



## PCH Strapping

Calpella Schematic Checklist Rev: 1.6

Name	Schematics Notes
SPKR	<b>Reboot option at power-up</b> <b>Default Mode:</b> Internal weak Pull-down. <b>No Reboot Mode with TCO Disabled:</b> Connect to Vcc3_3 with 8.2-kΩ ~ 10-kΩ weak pull-up resistor.
INIT3_3V#	Internal pull-up. Leave as "No Connect"
GNT3#/GPIO55	<b>Default Mode:</b> Internal pull-up. <b>Low (0) = Top Block Swap Mode</b> <b>Note:</b> Connect to ground with 4.7-kΩ weak pull-down resistor. CRB uses a 1 kΩ ; do not stuff resistor
INTVRMEN	<b>High (1) = Integrated VRM is enabled</b> <b>Low (0) = Integrated VRM is disabled</b> <b>Note:</b> CRB uses a 330-k resistor.
GNT0#, GNT1#	<b>Default (SPI):</b> Leave both GNT0# and GNT1# floating. No pull up required <b>Boot from PCI:</b> Connect GNT1# to ground with 1-kΩ pull-down resistor. Leave GNT0# Floating.  <b>Boot from LPC:</b> Connect both GNT0# and GNT1# to ground with 1-kΩ pull-down resistor.
GNT2#/GPIO53	<b>Default</b> - Internal pull-up. <b>Low (0)</b> = Configures DMI for ESI compatible operation (for servers only. Not for mobile/desktops).
SPI_MOSI	<b>Enable Intel Anti-Theft Technology:</b> Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor. <b>Disable Intel Anti-Theft Technology:</b> Left floating, no pull-down required.
NV_ALE	<b>Enable Intel Anti-Theft Technology:</b> Connect to +NVRAM_VCCQ with 8.2-kΩ weak pull-up resistor [CRB has it pulled up with 1-kΩ no-stuff resistor] <b>Disable Intel Anti-Theft Technology:</b> Leave floating (internal pull-down).
NV_CLE	DMI termination voltage. Weak internal pull-up. Do not pull low.
HDA_DOCK_EN# /GPIO[33]	<b>Low (0):</b> Flash Descriptor Security will be overridden. Also, when this signals is sampled on the rising edge of PWROK then it will also disable Intel ME and its features. <b>High (1):</b> Security measure defined in the Flash Descriptor will be enabled. Platform design should provide appropriate pull-up or pull-down depending on the desired settings. If a jumper option is used to tie this signal to GND as required by the functional strap, the signal should be pulled low through a weak pull-down in order to avoid asserting HDA_DOCK_EN# inadvertently. <b>Note:</b> CRB recommends 1-kΩ pull-down for FD Override. There is an internal pull-up of 20 kΩ for HDA_DOCK_EN# which is only enabled at boot/reset for strapping functions.
HDA_SDO	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
HDA_SYNC	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
GPIO15	Low (1) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality. High (1) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with confidentiality. <b>Note:</b> This is an unmuxed signal. This signal has a weak internal pull-down of 20KΩ which is enabled when PWROK is low. Sampled at rising edge of RSMRST#. CRB has a 1K pull-up on this signal to +3.3VA rail.
GPIO8	Weak internal pull-up. Do not pull low. Sampled at rising edge of RSMRST#.
GPIO27	<b>Default</b> = Do not connect (floating). Internal pull-up. <b>High(1)</b> = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. <b>Low (0)</b> = Disables the VccVRM. Need to use on-board filter circuits for analog rails.

## Processor Strapping

Calpella Schematic Checklist Rev: 1.6

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[4]	<b>Embedded DisplayPort Presence</b>	<b>1:</b> Disabled - No Physical Display Port attached to Embedded DisplayPort. <b>0:</b> Enabled - An external Display Port device is connected to the Embedded Display Port.	1
CFG[3]	<b>PCI-Express Static Lane Reversal</b>	<b>1:</b> Normal Operation. <b>0:</b> Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	1
CFG[0]	<b>PCI-Express Configuration Select</b>	<b>1:</b> Single PCI-Express Graphics <b>0:</b> Bifurcation enabled	1


## PCIE Routing

LANE1	WWAN
LANE2	WLAN
LANE3	PCMCIA
LANE4	Express Card
LANE5	None
LANE6	10M/100M/1G LAN
LANE7	Not available for HM55
LANE8	Not available for HM55

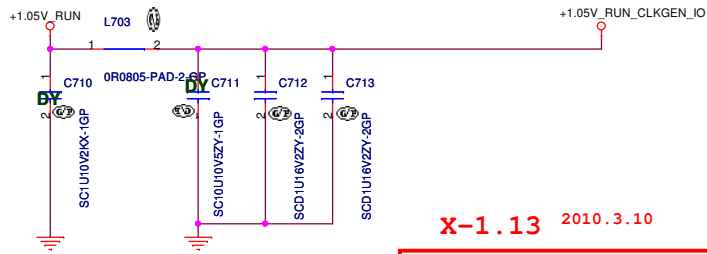
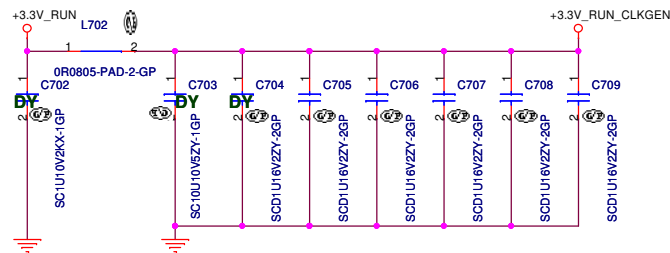
## USB Routing

USB	
Pair	Device
0	USB0 @ MB
1	USB1 @ MB
2	USB2 @ IO Board
3	USB3 @ IO Board
4	WLAN
5	Bluetooth
6	Not available for HM55
7	Not available for HM55
8	DOCKING PORT1
9	DOCKING PORT2
10	Finger Printer
11	Camera
12	PCCard / SmartCard
13	WWAN

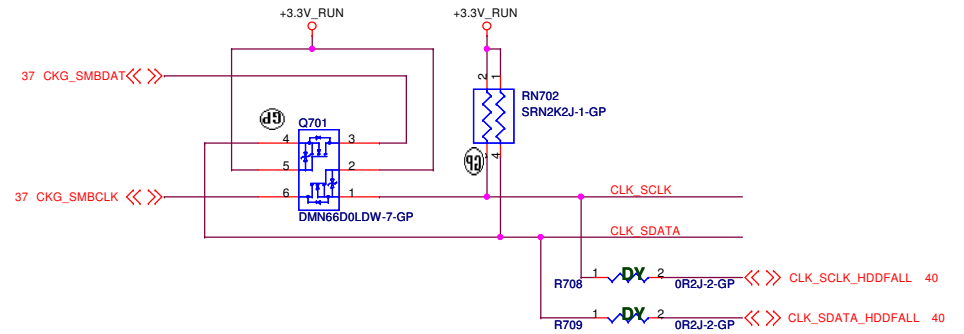
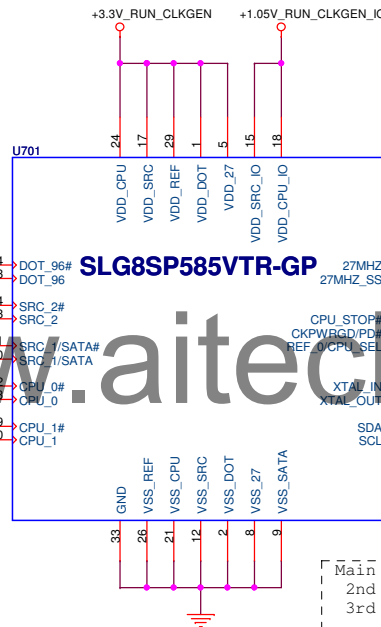
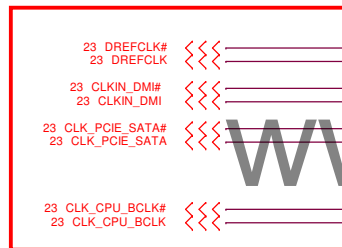
<Core Design>

		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
<b><i>Table of Content</i></b>			
Size A3	Document Number <b>Fonseca UMA</b>		Rev <b>X02</b>
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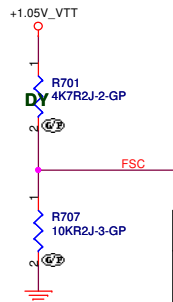
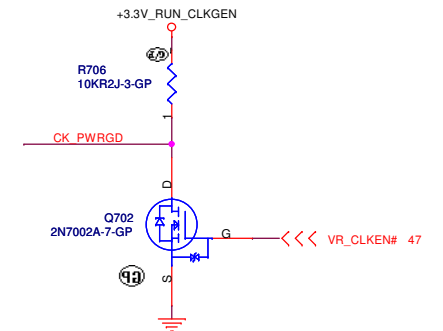
# SSID = CLOCK



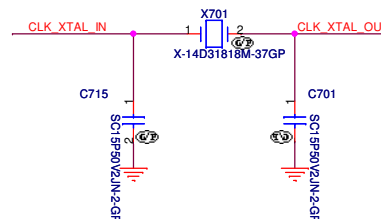
X-1.13 2010.3.10

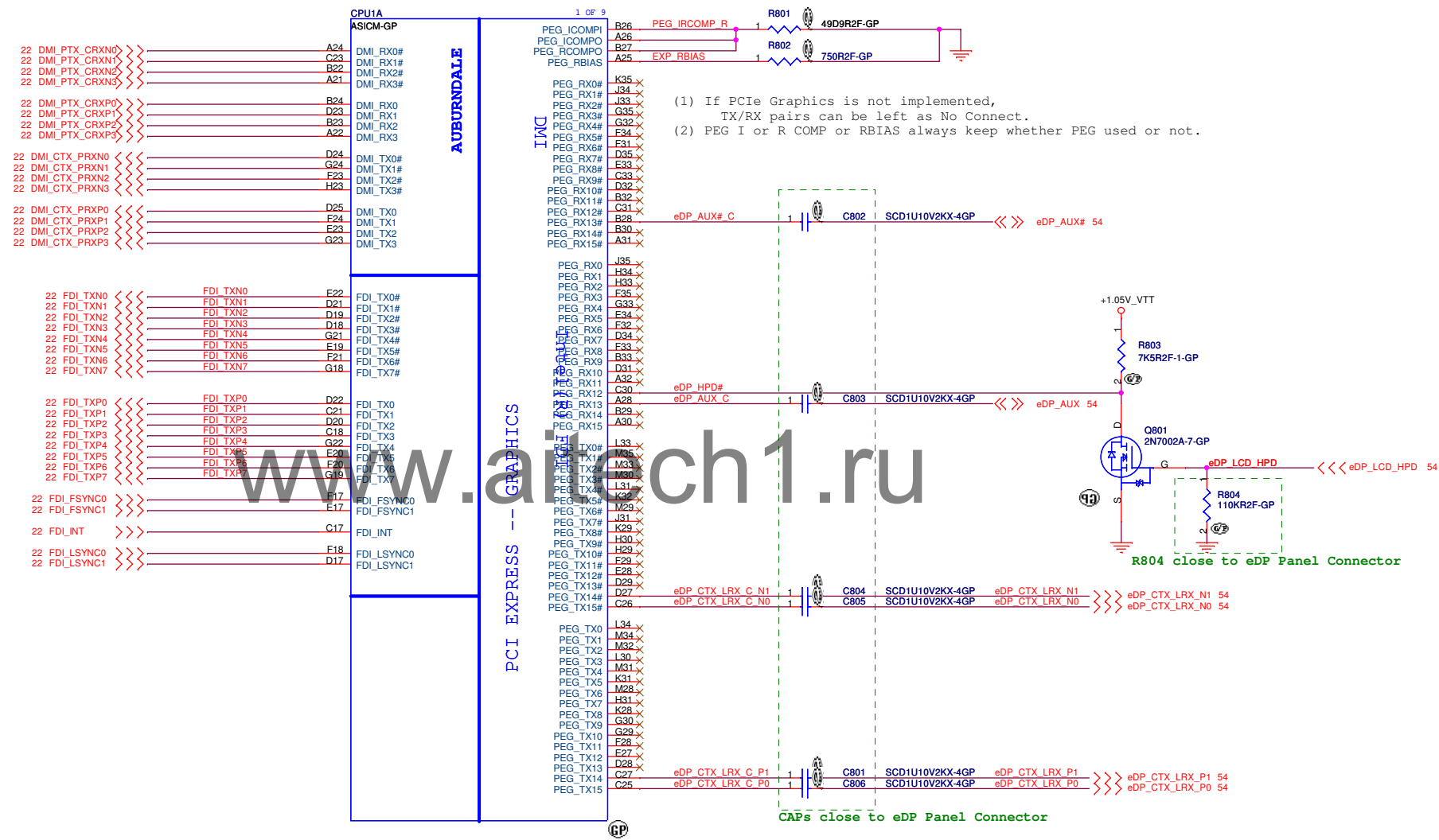


Main Source: 71.08585.003 (SLG8SP585VTR)  
2nd Source: 71.93197.003 (ICS9LRS3197AKLFT)  
3rd Source: 71.28748.A03 (SL28748ELCT)



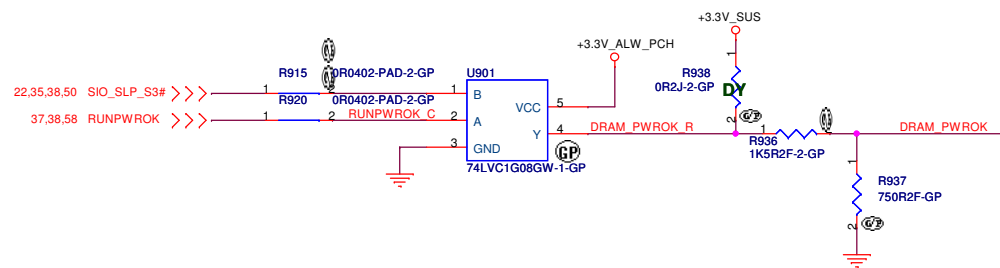
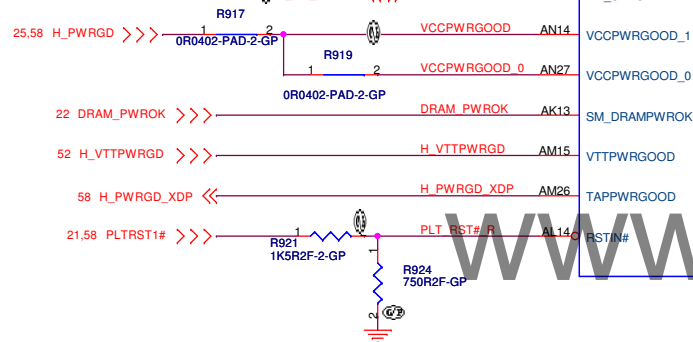
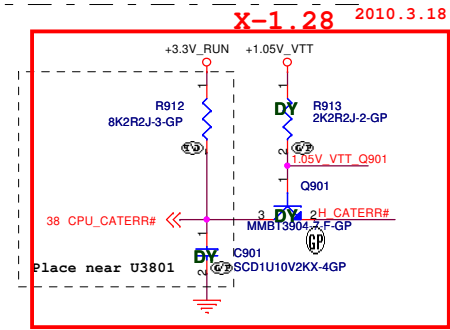
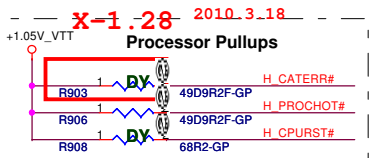
FSC	0	1
SPEED	133MHz (Default)	100MHz



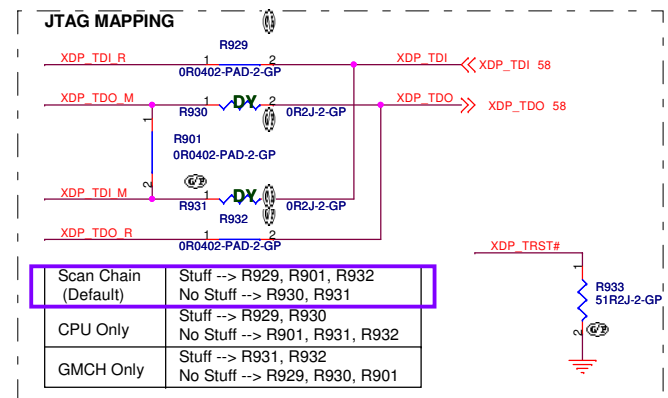
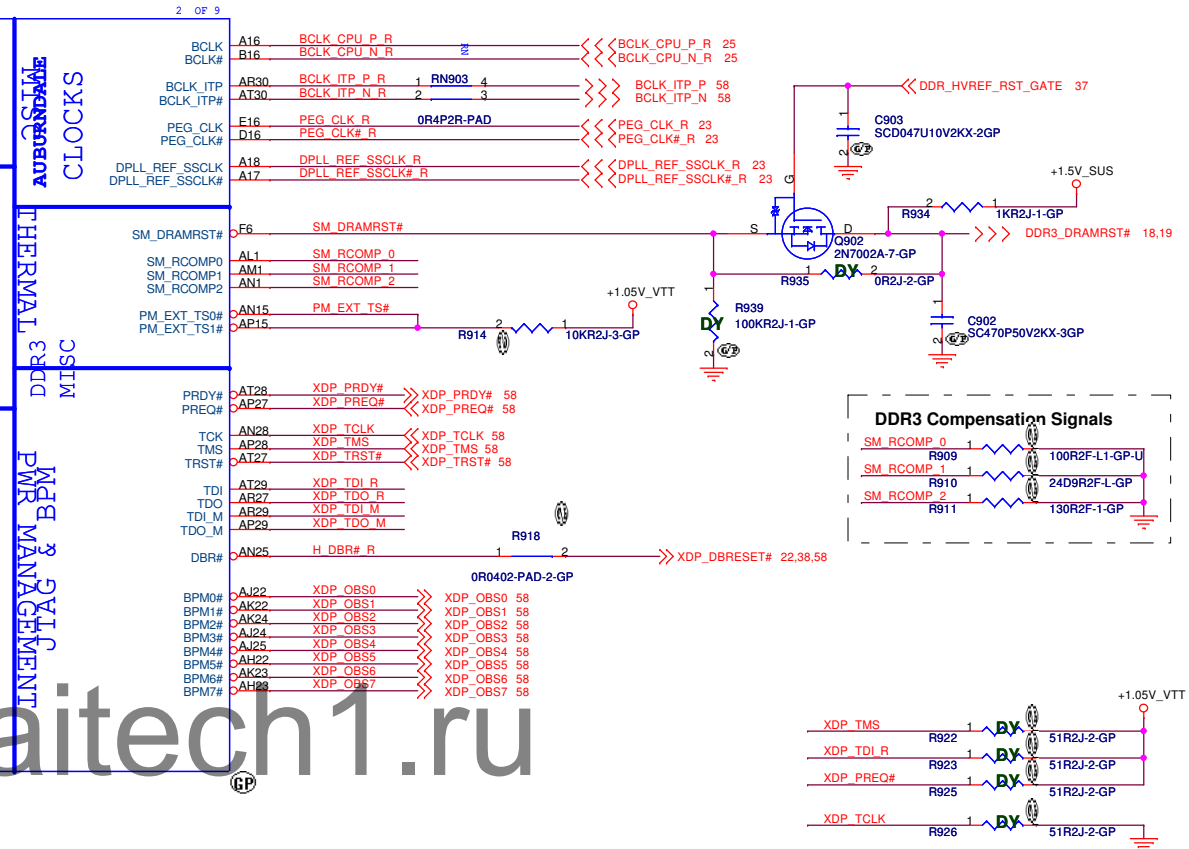


SSID = CPŮ

## Processor Compensation Signals



X01.09/0917



## <Core Design>



Title	<b>CPU Thermal/Clock/PM (2/7)</b>
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Size A3	Document Number <b>Fonseca UMA</b>	Rev <b>X02</b>
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SSID = CPU

CPU1C  
ASICM-GP

AUBURNDALE

DDR SYSTEM MEMORY A

3 OF 9

SA\_CK0  
SA\_CK0#  
SA\_CKE0

SA\_CK1  
SA\_CK1#  
SA\_CKE1

SA\_CS0#  
SA\_CS1#

SA\_ODT0  
SA\_ODT1

SA\_DM0  
SA\_DM1  
SA\_DM2  
SA\_DM3  
SA\_DM4  
SA\_DM5  
SA\_DM6  
SA\_DM7

SA\_DQS0#  
SA\_DQS1#  
SA\_DQS2#  
SA\_DQS3#  
SA\_DQS4#  
SA\_DQS5#  
SA\_DQS6#  
SA\_DQS7#

SA\_DQS0  
SA\_DQS1  
SA\_DQS2  
SA\_DQS3  
SA\_DQS4  
SA\_DQS5  
SA\_DQS6  
SA\_DQS7

SA\_MA0  
SA\_MA1  
SA\_MA2  
SA\_MA3  
SA\_MA4  
SA\_MA5  
SA\_MA6  
SA\_MA7  
SA\_MA8  
SA\_MA9  
SA\_MA10  
SA\_MA11  
SA\_MA12  
SA\_MA13  
SA\_MA14  
SA\_MA15

M\_CLK\_DDR0 18  
M\_CLK\_DDR#0 18  
M\_CKE0 18

M\_CLK\_DDR1 18  
M\_CLK\_DDR#1 18  
M\_CKE1 18

M\_CS#0 18  
M\_CS#1 18

M\_ODT0 18  
M\_ODT1 18

M\_A\_DM0  
M\_A\_DM1  
M\_A\_DM2  
M\_A\_DM3  
M\_A\_DM4  
M\_A\_DM5  
M\_A\_DM6  
M\_A\_DM7

M\_A\_DQS#0  
M\_A\_DQS#1  
M\_A\_DQS#2  
M\_A\_DQS#3  
M\_A\_DQS#4  
M\_A\_DQS#5  
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M\_A\_DQS#7

M\_A\_DQS0  
M\_A\_DQS1  
M\_A\_DQS2  
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M\_A\_DQS4  
M\_A\_DQS5  
M\_A\_DQS6  
M\_A\_DQS7

M\_A\_A0  
M\_A\_A1  
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M\_A\_A7  
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M\_A\_A9  
M\_A\_A10  
M\_A\_A11  
M\_A\_A12  
M\_A\_A13  
M\_A\_A14  
M\_A\_A15

M\_A\_BS0  
M\_A\_BS1  
M\_A\_BS2

M\_A\_CAS#  
M\_A\_RAS#  
M\_A\_WE#

19 M\_B\_DQ[63..0]

M\_B\_DQ0  
M\_B\_DQ1  
M\_B\_DQ2  
M\_B\_DQ3  
M\_B\_DQ4  
M\_B\_DQ5  
M\_B\_DQ6  
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M\_B\_DQ9  
M\_B\_DQ10  
M\_B\_DQ11  
M\_B\_DQ12  
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M\_B\_DQ54  
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M\_B\_DQ57  
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M\_B\_DQ10  
M\_B\_DQ11  
M\_B\_DQ12  
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M\_B\_DQ35  
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M\_B\_DQ37  
M\_B\_DQ38  
M\_B\_DQ39  
M\_B\_DQ40  
M\_B\_DQ41  
M\_B\_DQ42  
M\_B\_DQ43  
M\_B\_DQ44  
M\_B\_DQ45  
M\_B\_DQ46  
M\_B\_DQ47  
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M\_B\_DQ49  
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M\_B\_DQ51  
M\_B\_DQ52  
M\_B\_DQ53  
M\_B\_DQ54  
M\_B\_DQ55  
M\_B\_DQ56  
M\_B\_DQ57  
M\_B\_DQ58  
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M\_B\_DQ60  
M\_B\_DQ61  
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M\_B\_DQ63

M\_B\_DQ0  
M\_B\_DQ1  
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M\_B\_DQ9  
M\_B\_DQ10  
M\_B\_DQ11  
M\_B\_DQ12  
M\_B\_DQ13  
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M\_B\_DQ15  
M\_B\_DQ16  
M\_B\_DQ17  
M\_B\_DQ18  
M\_B\_DQ19  
M\_B\_DQ20  
M\_B\_DQ21  
M\_B\_DQ22  
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M\_B\_DQ24  
M\_B\_DQ25  
M\_B\_DQ26  
M\_B\_DQ27  
M\_B\_DQ28  
M\_B\_DQ29  
M\_B\_DQ30  
M\_B\_DQ31  
M\_B\_DQ32  
M\_B\_DQ33  
M\_B\_DQ34  
M\_B\_DQ35  
M\_B\_DQ36  
M\_B\_DQ37  
M\_B\_DQ38  
M\_B\_DQ39  
M\_B\_DQ40  
M\_B\_DQ41  
M\_B\_DQ42  
M\_B\_DQ43  
M\_B\_DQ44  
M\_B\_DQ45  
M\_B\_DQ46  
M\_B\_DQ47  
M\_B\_DQ48  
M\_B\_DQ49  
M\_B\_DQ50  
M\_B\_DQ51  
M\_B\_DQ52  
M\_B\_DQ53  
M\_B\_DQ54  
M\_B\_DQ55  
M\_B\_DQ56  
M\_B\_DQ57  
M\_B\_DQ58  
M\_B\_DQ59  
M\_B\_DQ60  
M\_B\_DQ61  
M\_B\_DQ62  
M\_B\_DQ63

M\_B\_DQ0  
M\_B\_DQ1  
M\_B\_DQ2  
M\_B\_DQ3  
M\_B\_DQ4  
M\_B\_DQ5  
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M\_B\_DQ7  
M\_B\_DQ8  
M\_B\_DQ9  
M\_B\_DQ10  
M\_B\_DQ11  
M\_B\_DQ12  
M\_B\_DQ13  
M\_B\_DQ14  
M\_B\_DQ15  
M\_B\_DQ16  
M\_B\_DQ17  
M\_B\_DQ18  
M\_B\_DQ19  
M\_B\_DQ20  
M\_B\_DQ21  
M\_B\_DQ22  
M\_B\_DQ23  
M\_B\_DQ24  
M\_B\_DQ25  
M\_B\_DQ26  
M\_B\_DQ27  
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M\_B\_DQ29  
M\_B\_DQ30  
M\_B\_DQ31  
M\_B\_DQ32  
M\_B\_DQ33  
M\_B\_DQ34  
M\_B\_DQ35  
M\_B\_DQ36  
M\_B\_DQ37  
M\_B\_DQ38  
M\_B\_DQ39  
M\_B\_DQ40  
M\_B\_DQ41  
M\_B\_DQ42  
M\_B\_DQ43  
M\_B\_DQ44  
M\_B\_DQ45  
M\_B\_DQ46  
M\_B\_DQ47  
M\_B\_DQ48  
M\_B\_DQ49  
M\_B\_DQ50  
M\_B\_DQ51  
M\_B\_DQ52  
M\_B\_DQ53  
M\_B\_DQ54  
M\_B\_DQ55  
M\_B\_DQ56  
M\_B\_DQ57  
M\_B\_DQ58  
M\_B\_DQ59  
M\_B\_DQ60  
M\_B\_DQ61  
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M\_B\_DQ63

M\_B\_DQ0  
M\_B\_DQ1  
M\_B\_DQ2  
M\_B\_DQ3  
M\_B\_DQ4  
M\_B\_DQ5  
M\_B\_DQ6  
M\_B\_DQ7  
M\_B\_DQ8  
M\_B\_DQ9  
M\_B\_DQ10  
M\_B\_DQ11  
M\_B\_DQ12  
M\_B\_DQ13  
M\_B\_DQ14  
M\_B\_DQ15  
M\_B\_DQ16  
M\_B\_DQ17  
M\_B\_DQ18  
M\_B\_DQ19  
M\_B\_DQ20  
M\_B\_DQ21  
M\_B\_DQ22  
M\_B\_DQ23  
M\_B\_DQ24  
M\_B\_DQ25  
M\_B\_DQ26  
M\_B\_DQ27  
M\_B\_DQ28  
M\_B\_DQ29  
M\_B\_DQ30  
M\_B\_DQ31  
M\_B\_DQ32  
M\_B\_DQ33  
M\_B\_DQ34  
M\_B\_DQ35  
M\_B\_DQ36  
M\_B\_DQ37  
M\_B\_DQ38  
M\_B\_DQ39  
M\_B\_DQ40  
M\_B\_DQ41  
M\_B\_DQ42  
M\_B\_DQ43  
M\_B\_DQ44  
M\_B\_DQ45  
M\_B\_DQ46  
M\_B\_DQ47  
M\_B\_DQ48  
M\_B\_DQ49  
M\_B\_DQ50  
M\_B\_DQ51  
M\_B\_DQ52  
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M\_B\_DQ54  
M\_B\_DQ55  
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M\_B\_DQ58  
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M\_B\_DQ63

M\_B\_DQ0  
M\_B\_DQ1  
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M\_B\_DQ3  
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M\_B\_DQ7  
M\_B\_DQ8  
M\_B\_DQ9  
M\_B\_DQ10  
M\_B\_DQ11  
M\_B\_DQ12  
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M\_B\_DQ16  
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M\_B\_DQ29  
M\_B\_DQ30  
M\_B\_DQ31  
M\_B\_DQ32  
M\_B\_DQ33  
M\_B\_DQ34  
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M\_B\_DQ36  
M\_B\_DQ37  
M\_B\_DQ38  
M\_B\_DQ39  
M\_B\_DQ40  
M\_B\_DQ41  
M\_B\_DQ42  
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M\_B\_DQ46  
M\_B\_DQ47  
M\_B\_DQ48  
M\_B\_DQ49  
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M\_B\_DQ51  
M\_B\_DQ52  
M\_B\_DQ53  
M\_B\_DQ54  
M\_B\_DQ55  
M\_B\_DQ56  
M\_B\_DQ57  
M\_B\_DQ58  
M\_B\_DQ59  
M\_B\_DQ60  
M\_B\_DQ61  
M\_B\_DQ62  
M\_B\_DQ63

M\_B\_DQ0  
M\_B\_DQ1  
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M\_B\_DQ3  
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M\_B\_DQ5  
M\_B\_DQ6  
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M\_B\_DQ8  
M\_B\_DQ9  
M\_B\_DQ10  
M\_B\_DQ11  
M\_B\_DQ12  
M\_B\_DQ13  
M\_B\_DQ14  
M\_B\_DQ15  
M\_B\_DQ16  
M\_B\_DQ17  
M\_B\_DQ18  
M\_B\_DQ19  
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M\_B\_DQ25  
M\_B\_DQ26  
M\_B\_DQ27  
M\_B\_DQ28  
M\_B\_DQ29  
M\_B\_DQ30  
M\_B\_DQ31  
M\_B\_DQ32  
M\_B\_DQ33  
M\_B\_DQ34  
M\_B\_DQ35  
M\_B\_DQ36  
M\_B\_DQ37  
M\_B\_DQ38  
M\_B\_DQ39  
M\_B\_DQ40  
M\_B\_DQ41  
M\_B\_DQ42  
M\_B\_DQ43  
M\_B\_DQ44  
M\_B\_DQ45  
M\_B\_DQ46  
M\_B\_DQ47  
M\_B\_DQ48  
M\_B\_DQ49  
M\_B\_DQ50  
M\_B\_DQ51  
M\_B\_DQ52  
M\_B\_DQ53  
M\_B\_DQ54  
M\_B\_DQ55  
M\_B\_DQ56  
M\_B\_DQ57  
M\_B\_DQ58  
M\_B\_DQ59  
M\_B\_DQ60  
M\_B\_DQ61  
M\_B\_DQ62  
M\_B\_DQ63

M\_B\_BS0  
M\_B\_BS1  
M\_B\_BS2

M\_B\_CAS#  
M\_B\_RAS#  
M\_B\_WE#

CPU1D  
ASICM-GP

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DDR SYSTEM MEMORY - B

4 OF 9

SB\_CK0  
SB\_CK0#  
SB\_CKE0

SB\_CK1  
SB\_CK1#  
SB\_CKE1

SB\_CS0#  
SB\_CS1#

SB\_ODT0  
SB\_ODT1

SB\_DM0  
SB\_DM1  
SB\_DM2  
SB\_DM3  
SB\_DM4  
SB\_DM5  
SB\_DM6  
SB\_DM7

SB\_DQS0#  
SB\_DQS1#  
SB\_DQS2#  
SB\_DQS3#  
SB\_DQS4#  
SB\_DQS5#  
SB\_DQS6#  
SB\_DQS7#

SB\_DQS0  
SB\_DQS1  
SB\_DQS2  
SB\_DQS3  
SB\_DQS4  
SB\_DQS5  
SB\_DQS6  
SB\_DQS7

SB\_MA0  
SB\_MA1  
SB\_MA2  
SB\_MA3  
SB\_MA4  
SB\_MA5  
SB\_MA6  
SB\_MA7  
SB\_MA8  
SB\_MA9  
SB\_MA10  
SB\_MA11  
SB\_MA12  
SB\_MA13  
SB\_MA14  
SB\_MA15

W8  
W9  
M3

V7  
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AB8  
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D4  
E1  
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AL2  
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D5  
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AR5  
AR8

C5  
E3  
H4  
M5  
AG2  
AL5  
AP5  
AR7

U5  
V2  
T5  
V3  
R1  
T8  
R2  
R6  
R4  
R5  
R5  
P3  
R3  
AF7  
P5  
N1

M\_B\_DQ0  
M\_B\_DQ1  
M\_B\_DQ2  
M\_B\_DQ3  
M\_B\_DQ4  
M\_B\_DQ5  
M\_B\_DQ6  
M\_B\_DQ7

M\_B\_DQ0  
M\_B\_DQ1  
M\_B\_DQ2  
M\_B\_DQ3  
M\_B\_DQ4  
M\_B\_DQ5  
M\_B\_DQ6  
M\_B\_DQ7

M\_B\_DQ0  
M\_B\_DQ1  
M\_B\_DQ2  
M\_B\_DQ3  
M\_B\_DQ4  
M\_B\_DQ5  
M\_B\_DQ6  
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M\_B\_DQ0  
M\_B\_DQ1  
M\_B\_DQ2  
M\_B\_DQ3  
M\_B\_DQ4  
M\_B\_DQ5  
M\_B\_DQ6  
M\_B\_DQ7

M\_B\_DQ0  
M\_B\_DQ1  
M\_B\_DQ2  
M\_B\_DQ3  
M\_B\_DQ4  
M\_B\_DQ5  
M\_B\_DQ6  
M\_B\_DQ7

M\_B\_DQ0  
M\_B\_DQ1  
M\_B\_DQ2  
M\_B\_DQ3  
M\_B\_DQ4  
M\_B\_DQ5  
M\_B\_DQ6  
M\_B\_DQ7

<Core Design>

GP

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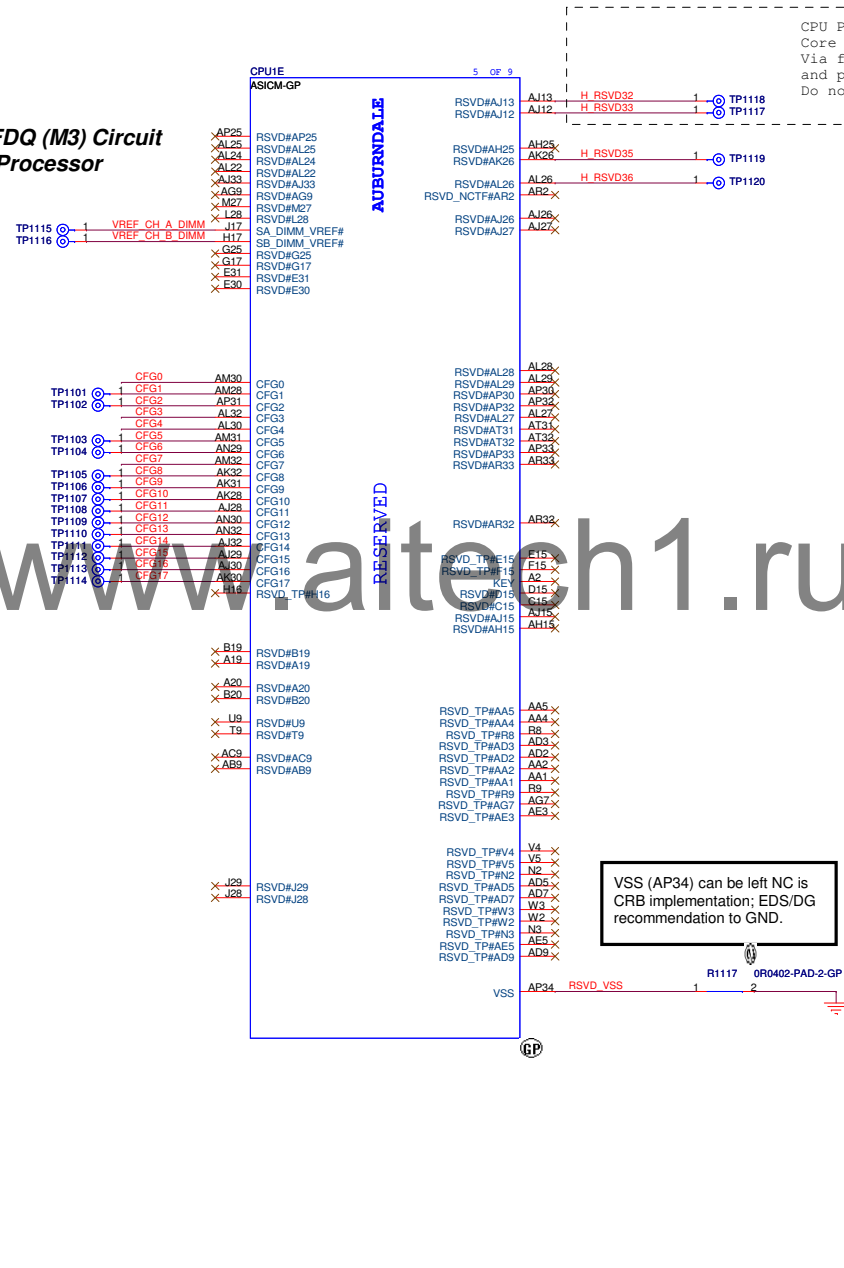
Title  
**CPU - DDR (3/7)**

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SSID = CPU

### SO-DIMM VREFDQ (M3) Circuit for Clarkfield Processor



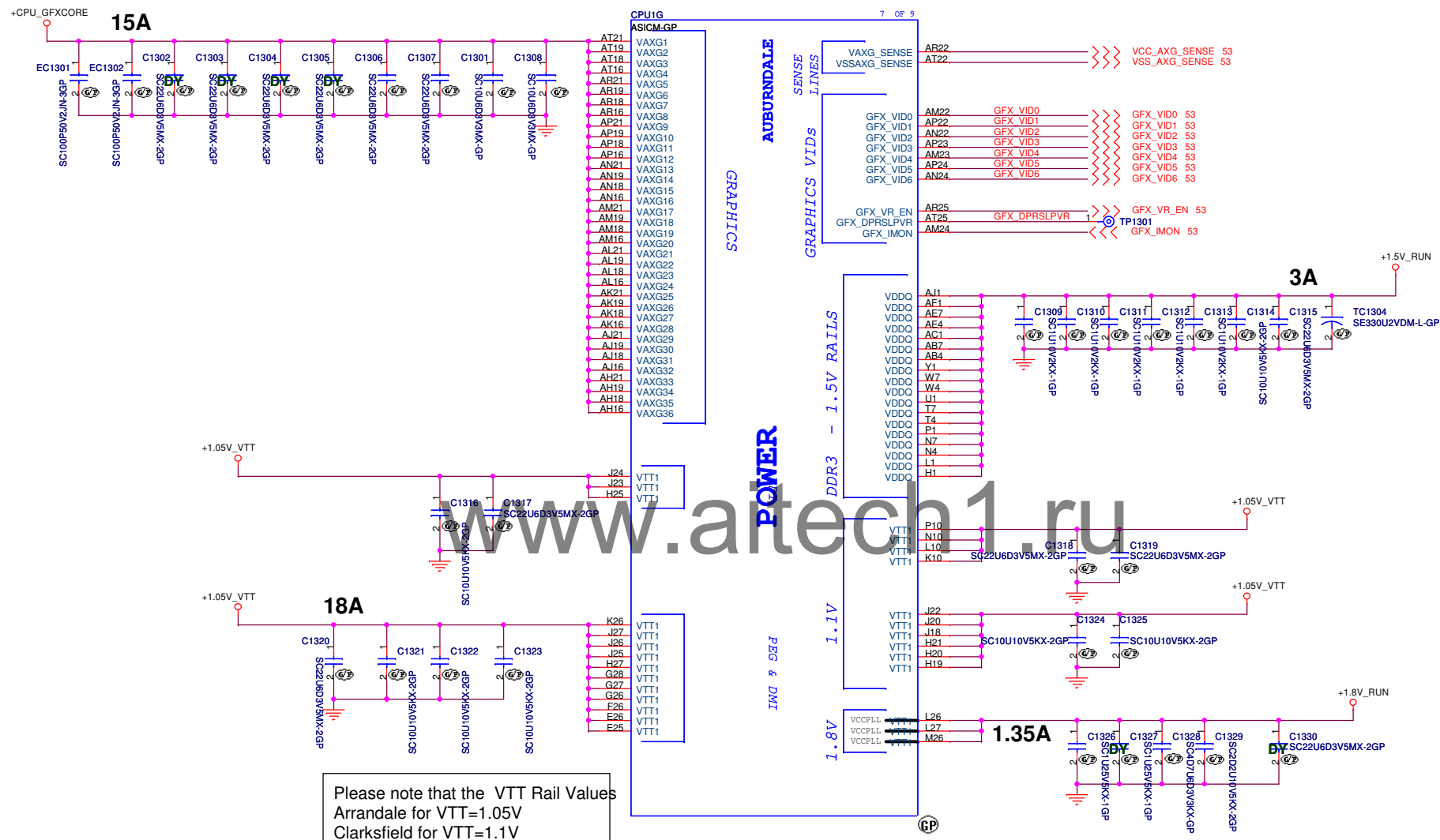
<Core Design>





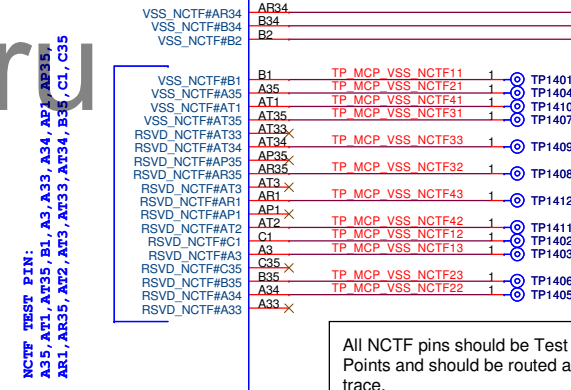
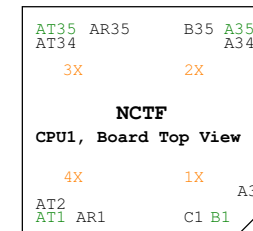
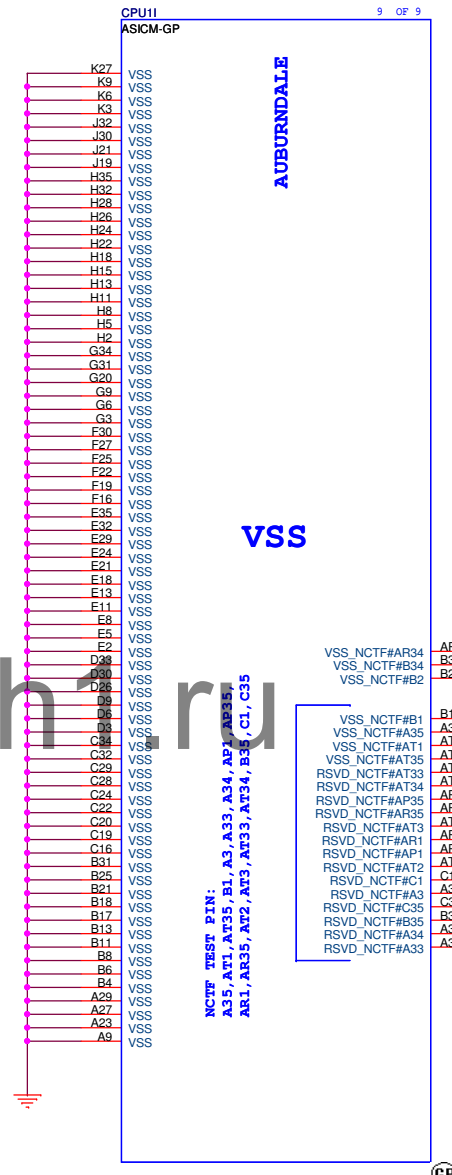
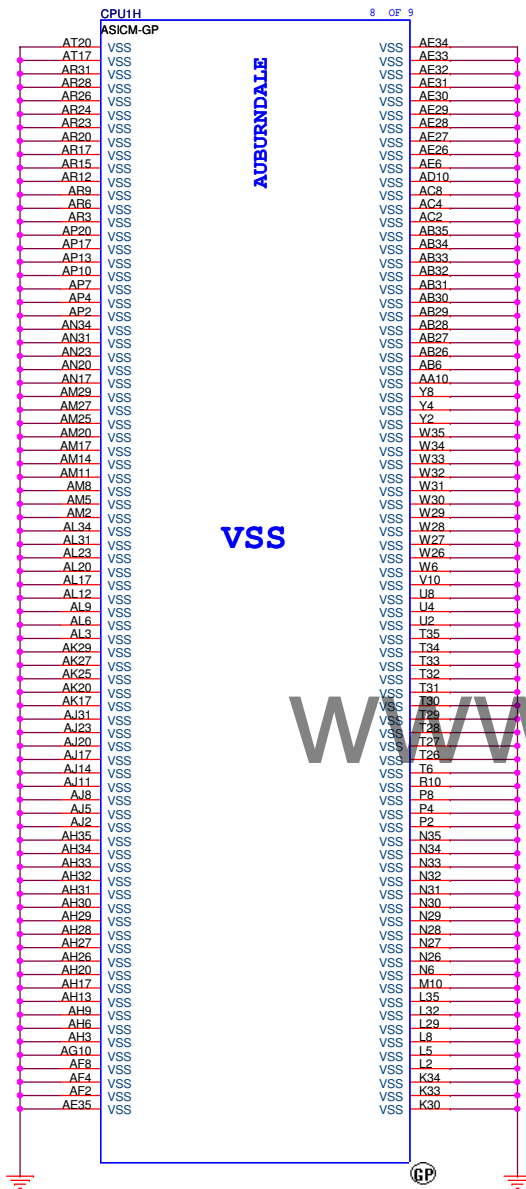


**SSID = CPU**



Please note that the VTT Rail Values  
Arrandale for VTT=1.05V  
Clarksfield for VTT=1.1V


SSID = CPU



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**Reserve**


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**Reserve**


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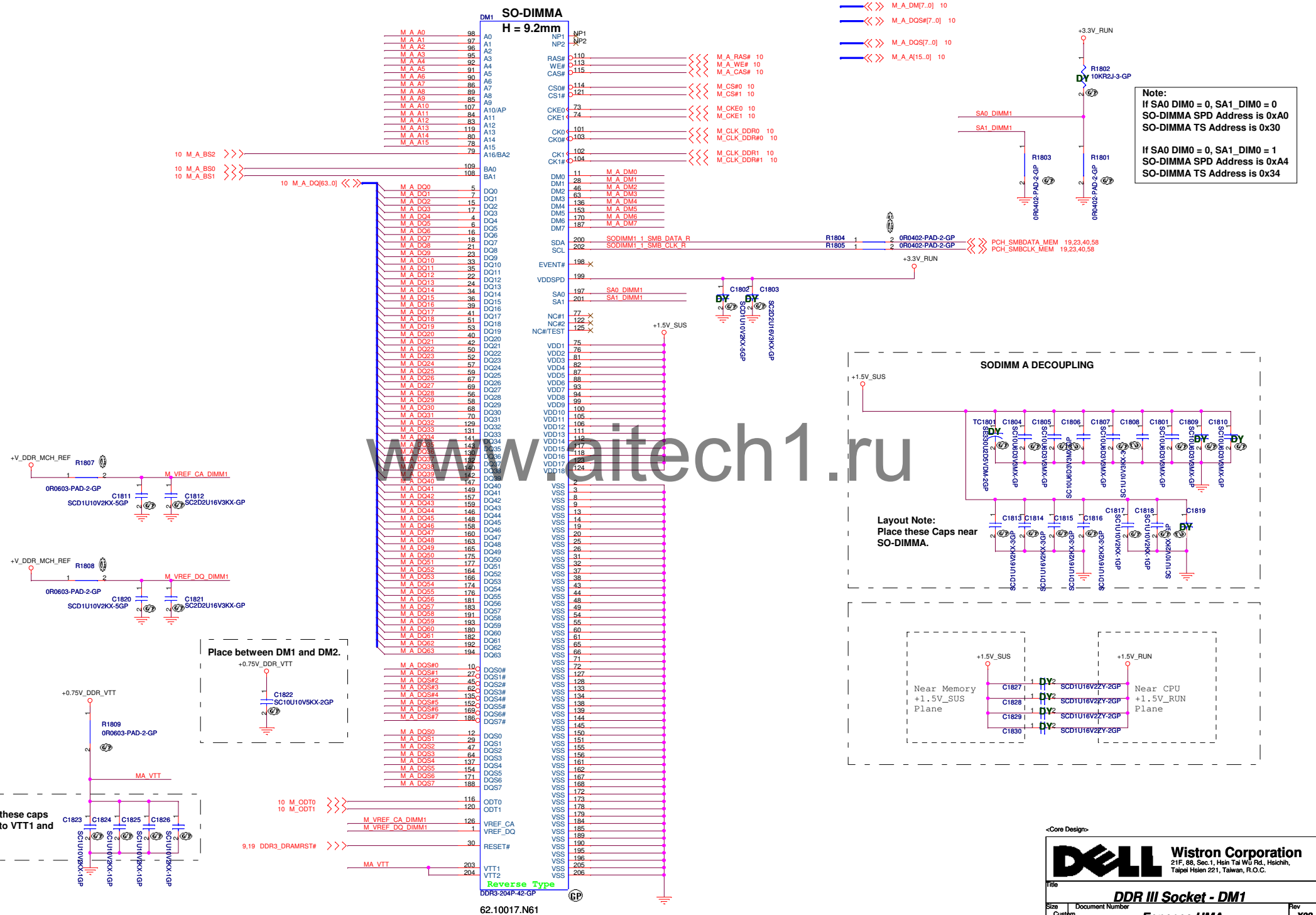
Title

**Reserve**

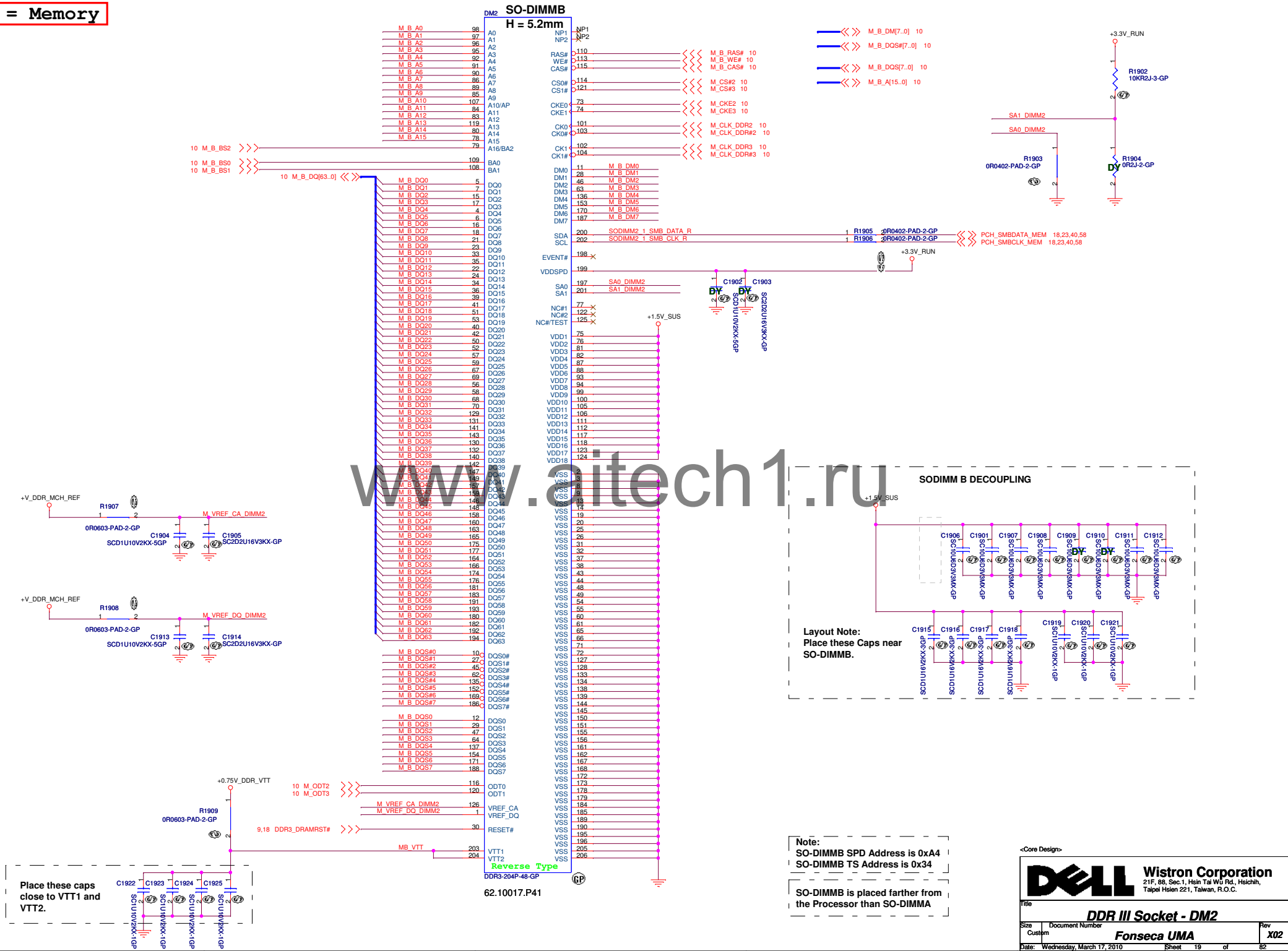
Size	Document Number	Rev
Custom	<b>Fonseca UMA</b>	<b>X02</b>

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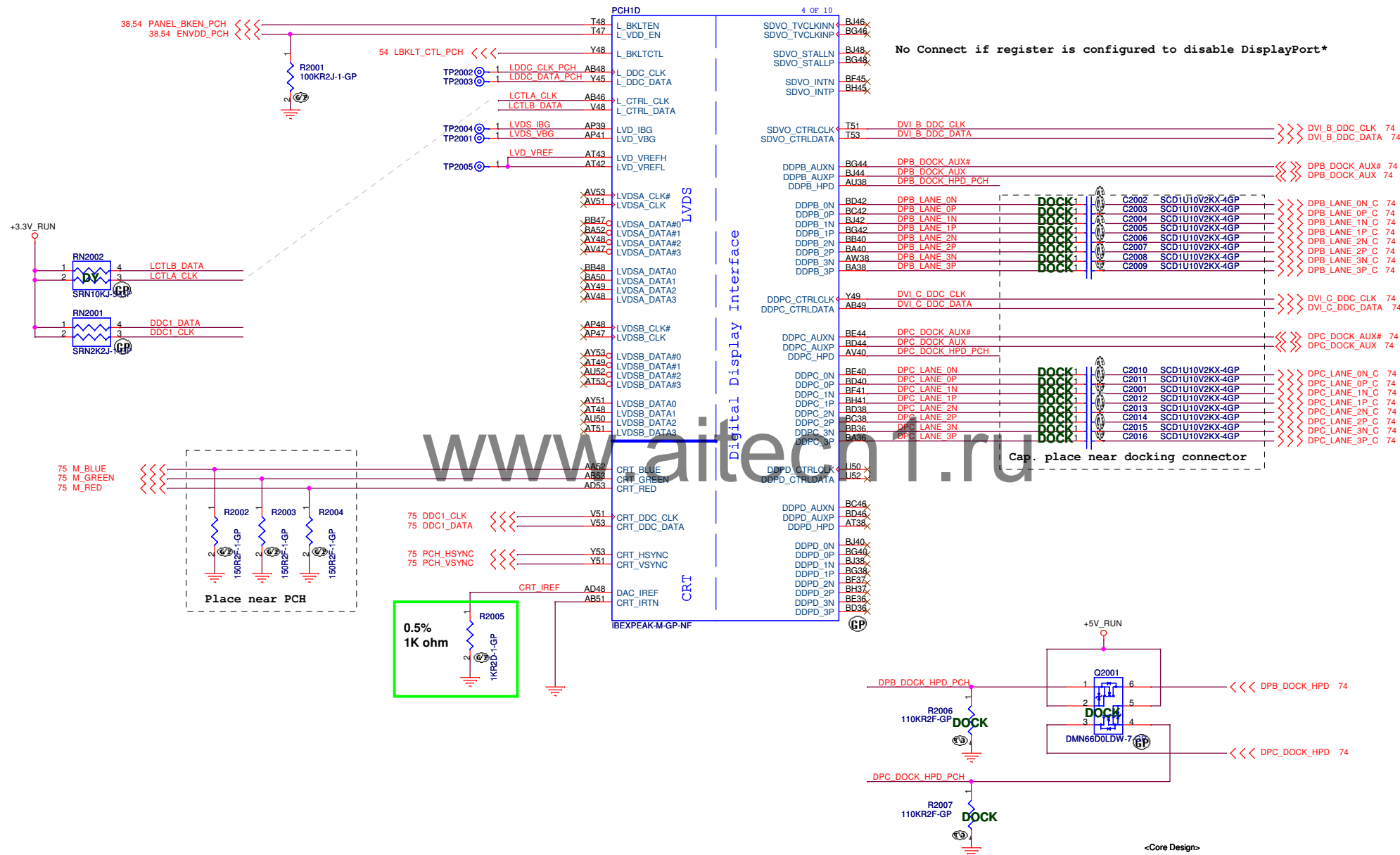
**SSID = Memory**



**SSID = Memory**



**SSID = PCH**



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### PCH - LVDS/CRT/DDI (1/9)

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**Fonseca UMA**

Rev  
**X02**

Date: Thursday, March 18, 2010

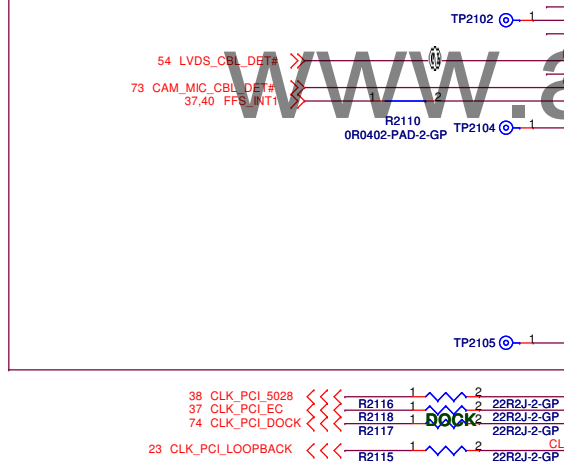
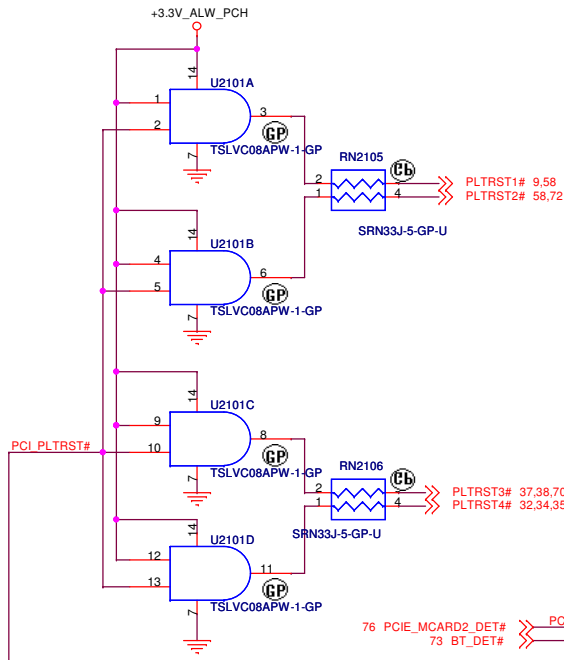
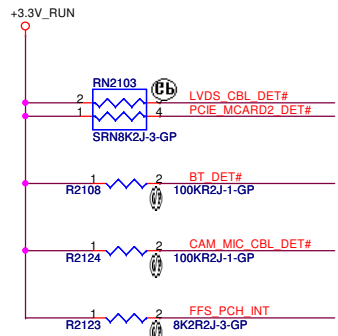
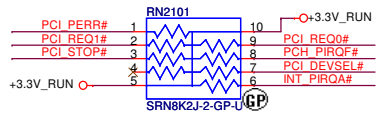
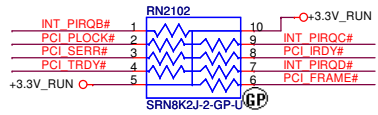
Sheet 20

---

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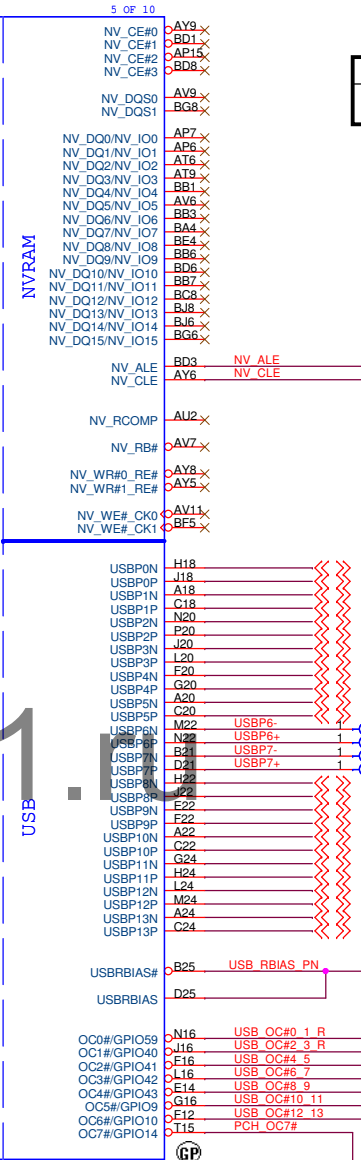
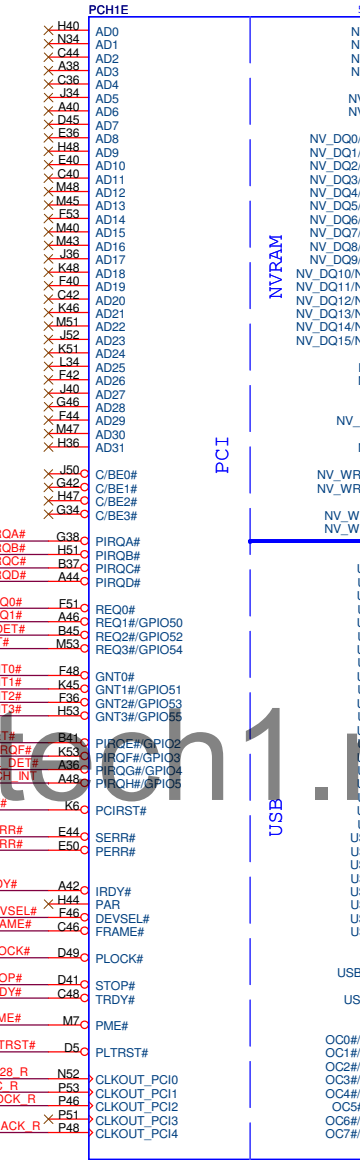
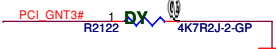


# SSID = PCH



BOOT BIOS Strap		
PCI_GNT#0	PCI_GNT#1	BOOT BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI(Default)

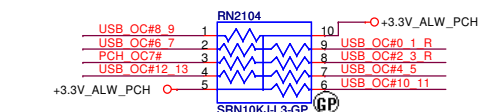
PCI\_GNT[3:0]#: Internal pull high during Strap



DMI Termination Voltage	
NV_CLE	Set to Vss when low. Set to Vcc when high.

Danbury Technology:  
Disabled when Low.  
Enable when High.

USB	
Pair	Device
0	USB0 @ MB (Charger)
1	USB1 @ MB
2	USB2 @ IO Board
3	USB3 @ IO Board
4	WLAN
5	Bluetooth
6	Not available for HM55
7	Not available for HM55
8	DOCK1
9	DOCK2
10	Finger Printer
11	Camera
12	PCCard / SmartCard
13	WWAN



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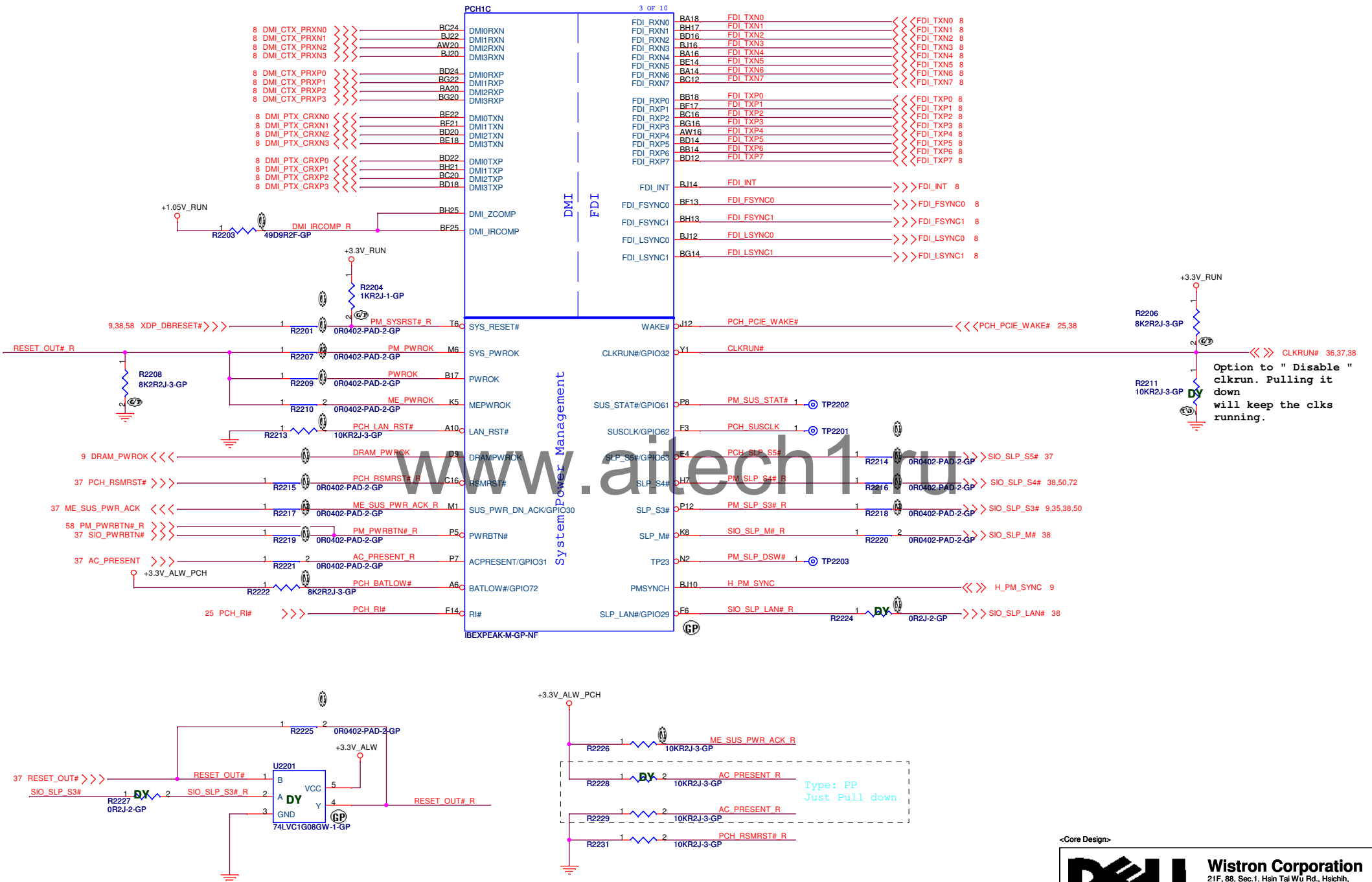
File

**PCH - PCI/USB/NVRAM (2/9)**

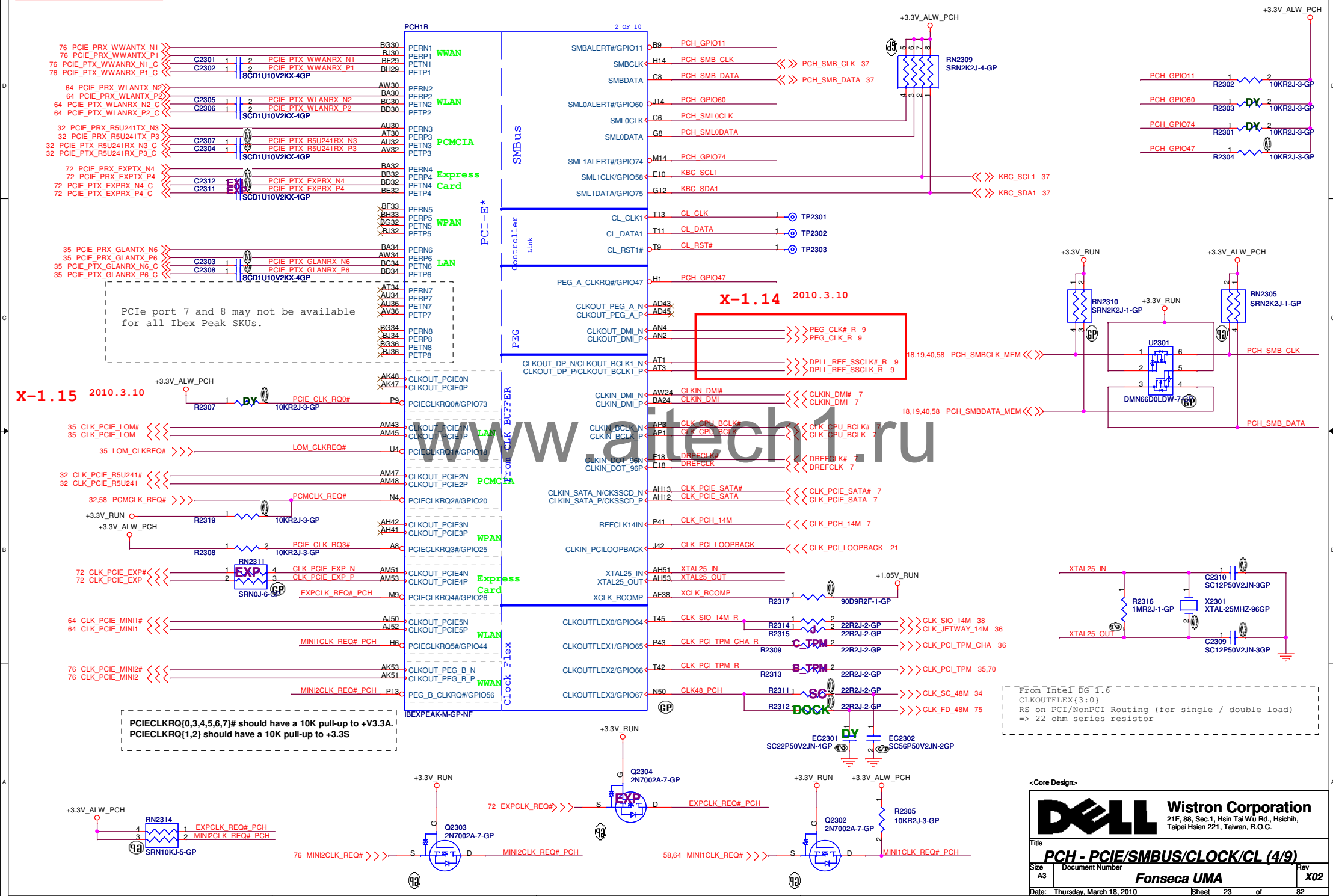
Size A3 Document Number **Fonseca UMA** Rev **X02**

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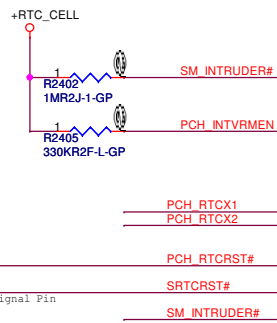
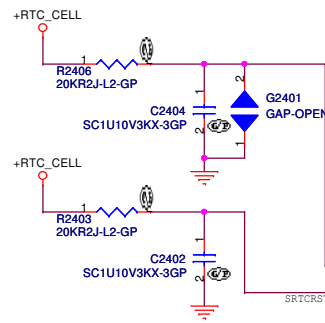
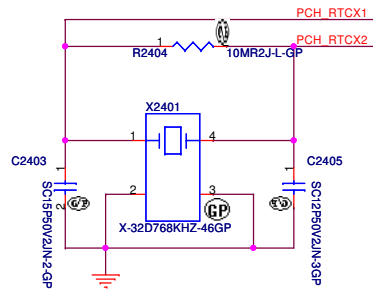
SSID = PCH



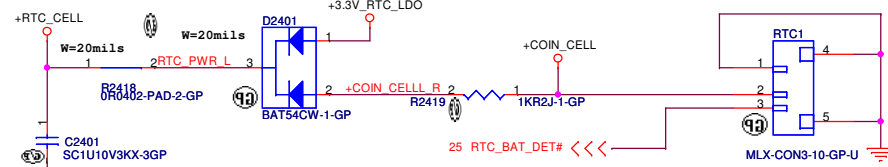
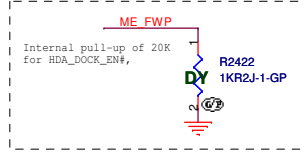
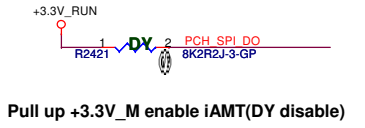
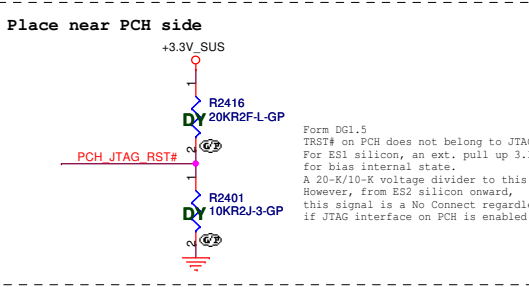
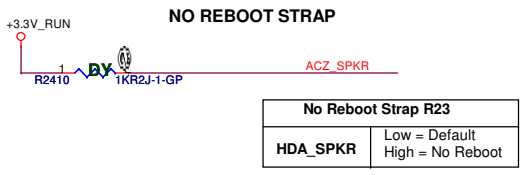
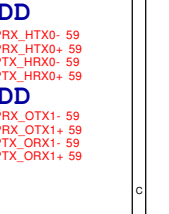
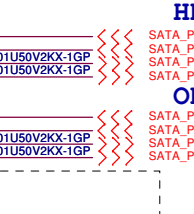
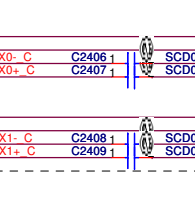
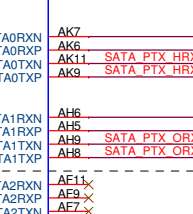
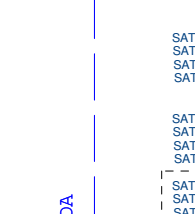
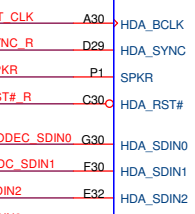
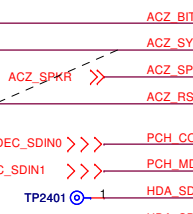
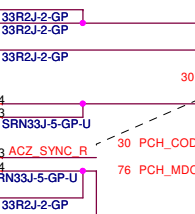
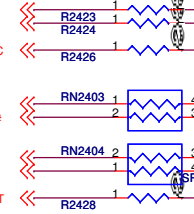
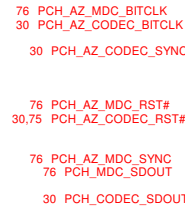
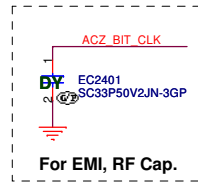
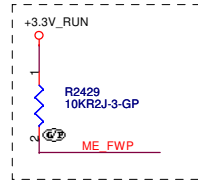
**SSID = PCH**



**SSID = PCH**

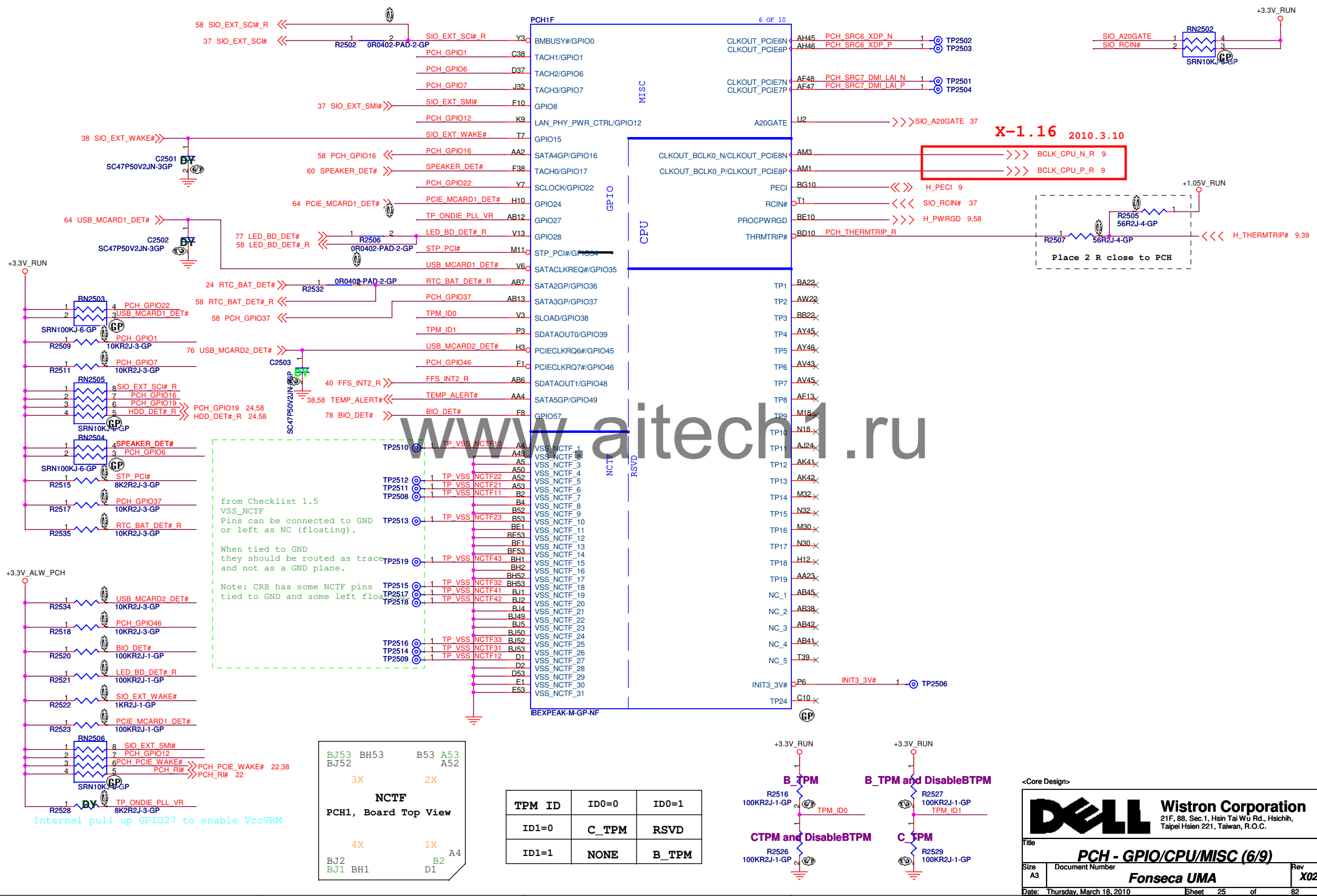


INTVRMEN- Integrated SUS  
1.1V VRM Enable  
High - Enable internal VRs

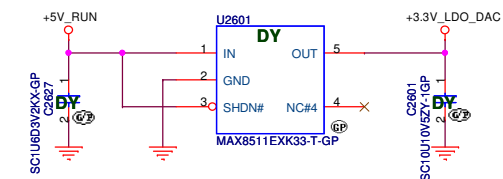
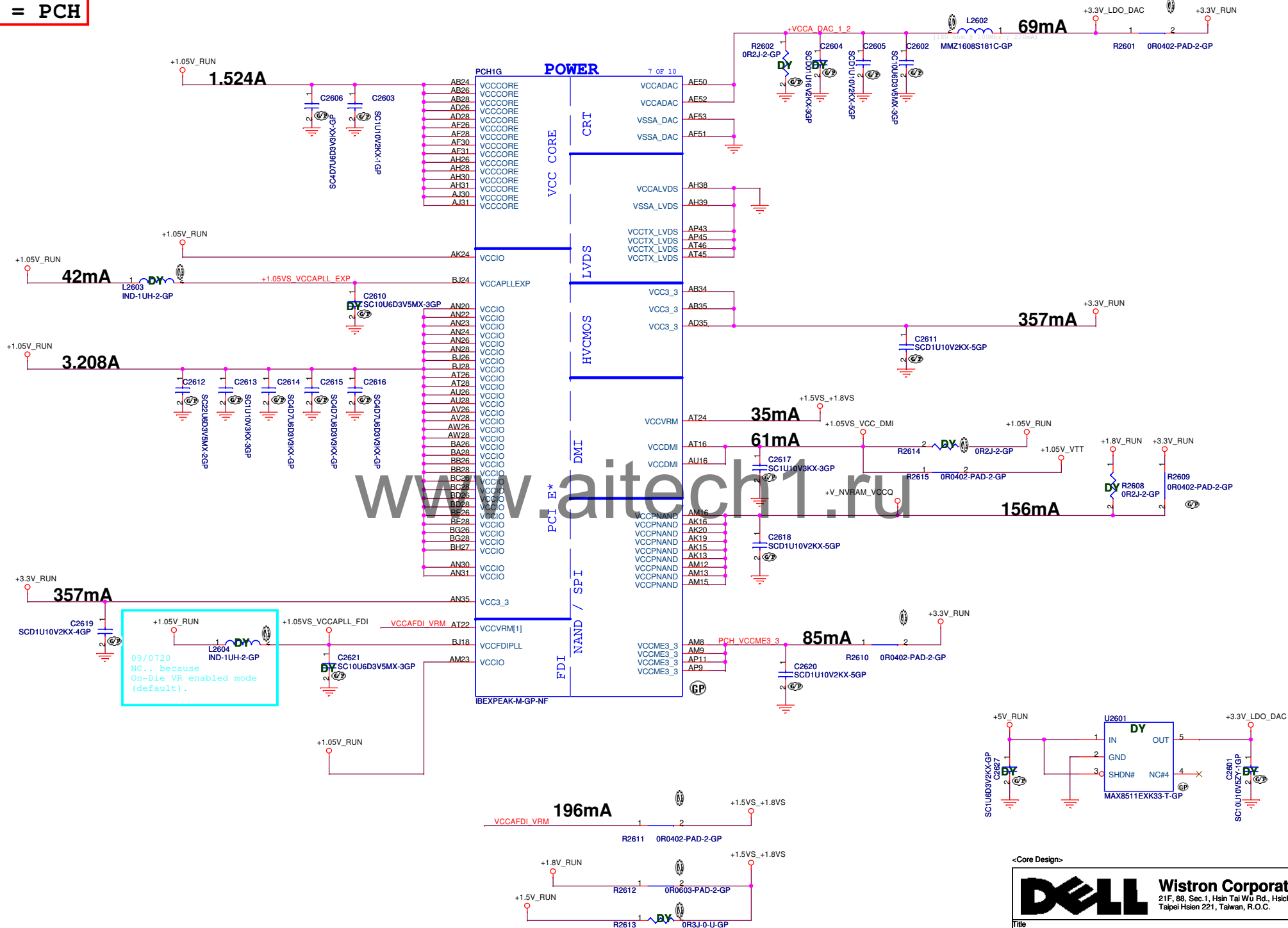


integrated VccSns1_05,VccSns1_5,VccCL1_5	
INTVRMEN	High=Enable Low=Disable
integrated VccLan1_05VccCL1_05	
LAN100_SLP	High=Enable Low=Disable

## SSID = PCH

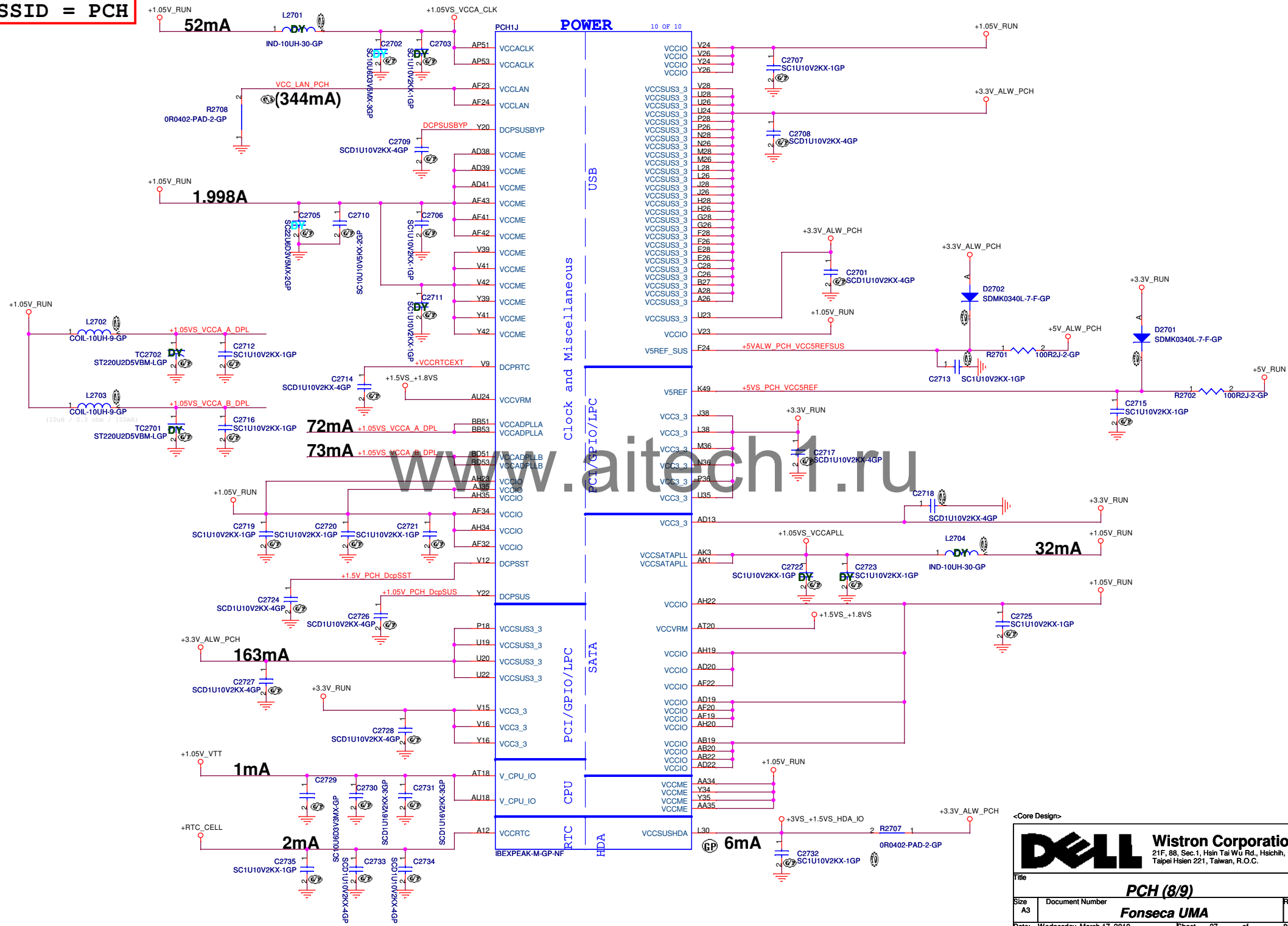


**SSID = PCH**

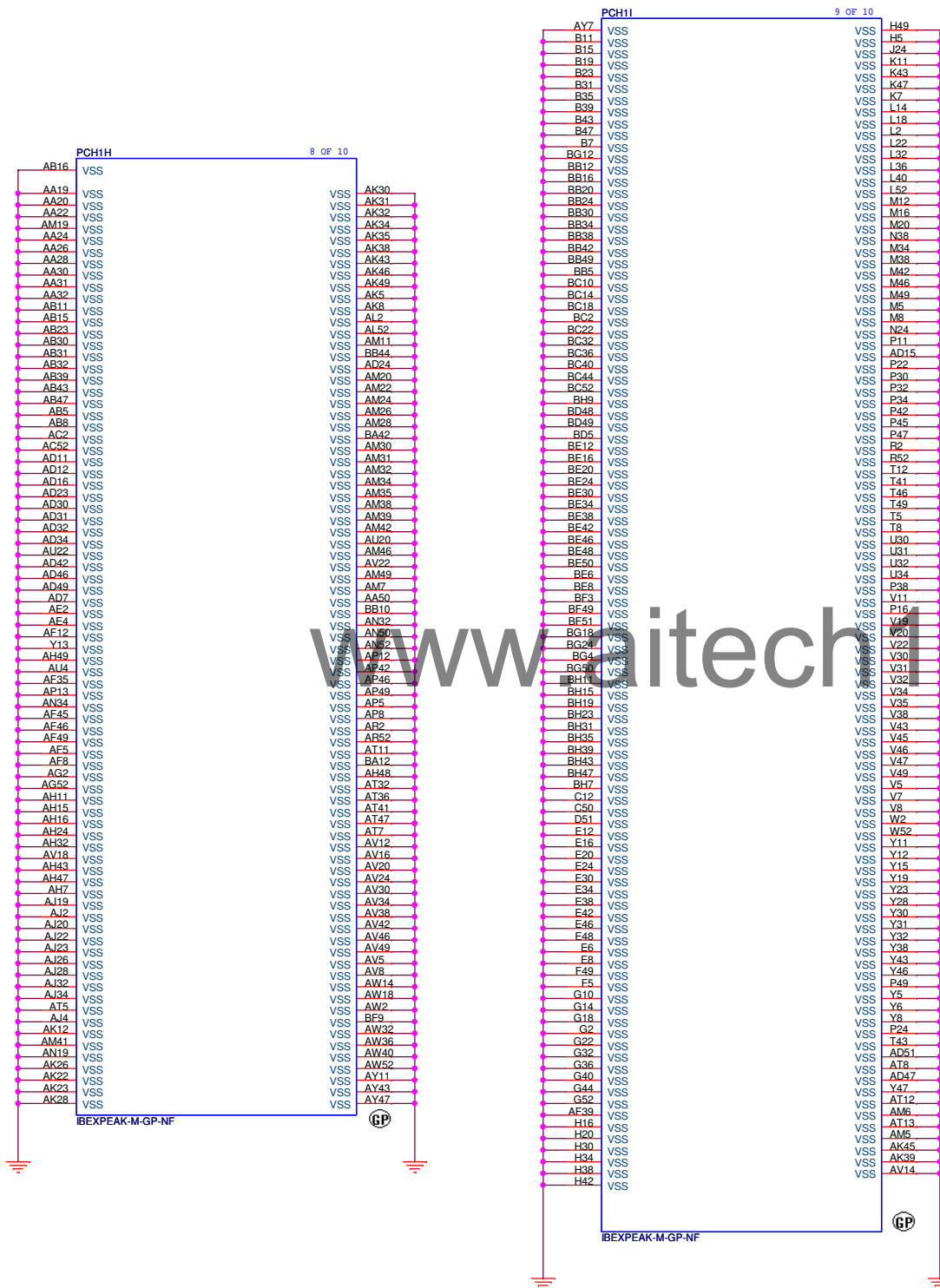




**SSID = PCH**



SSID = PCH






(Blank)

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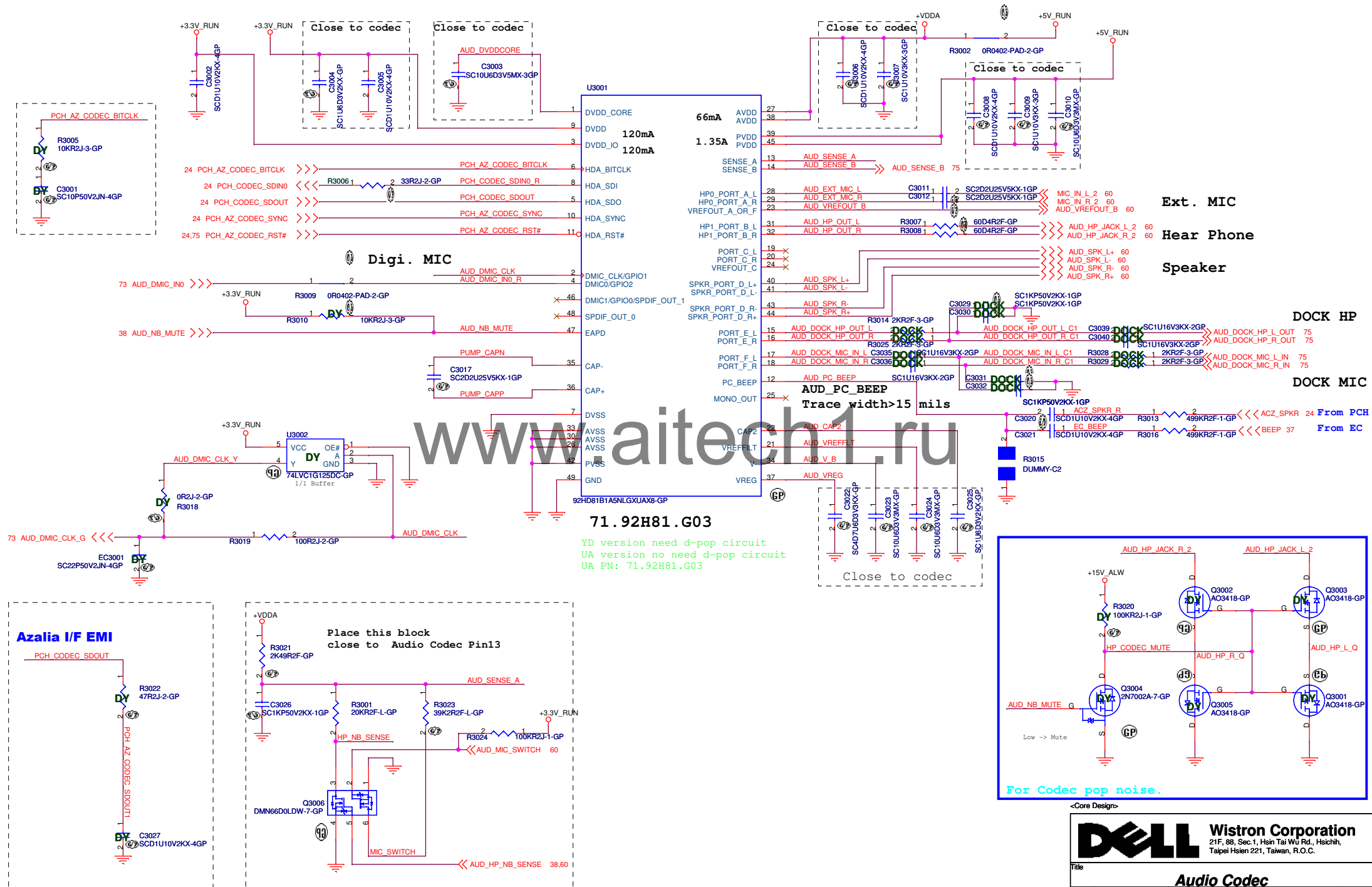
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X02

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# SSID = AUDIO



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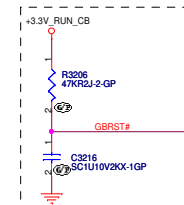
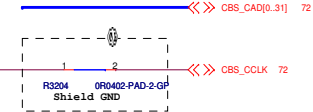
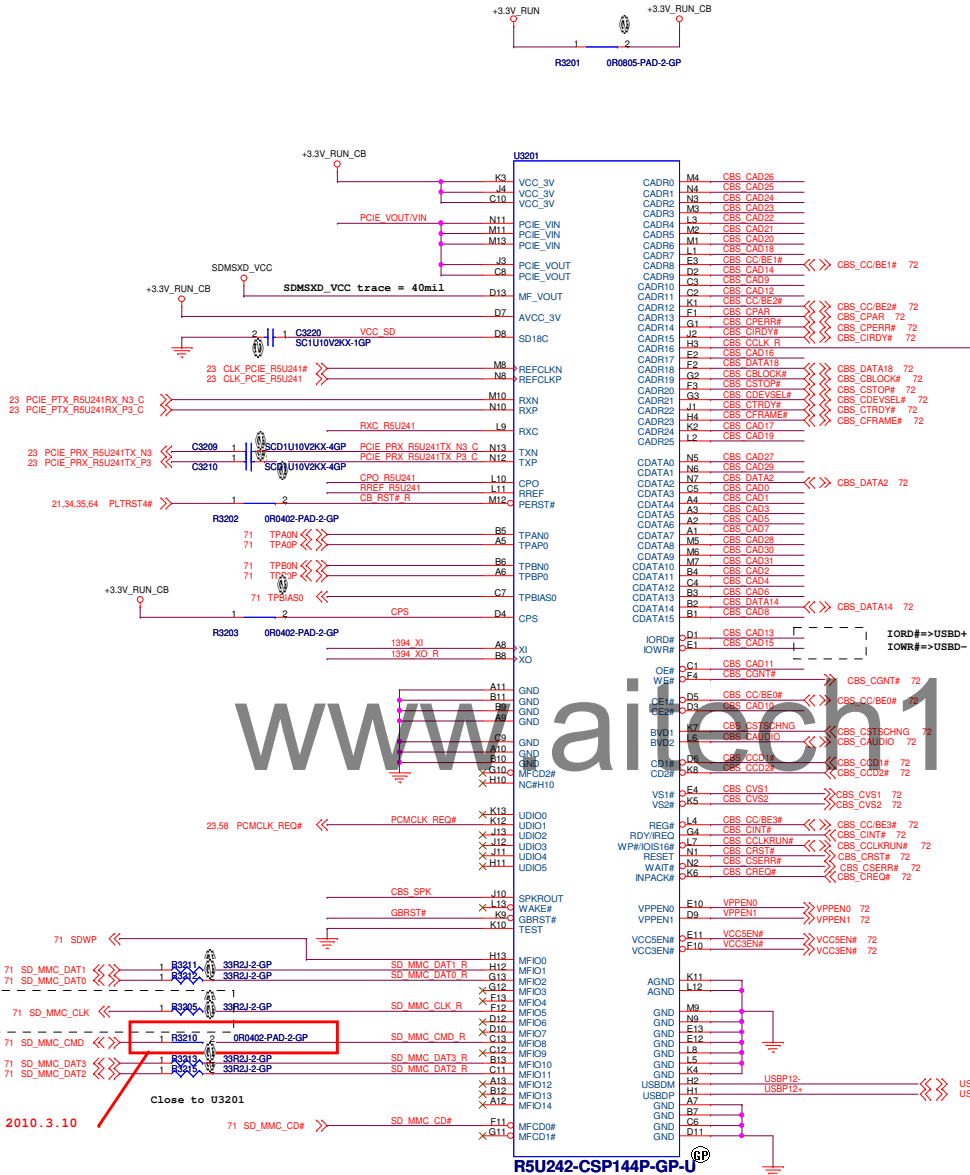
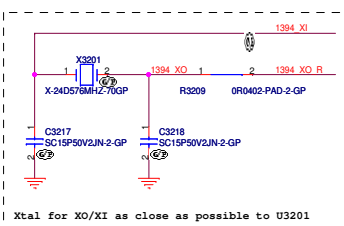
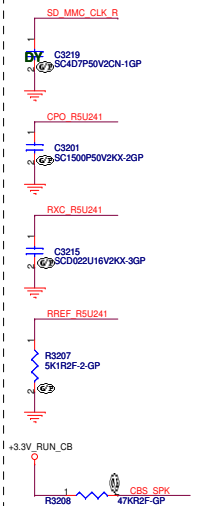
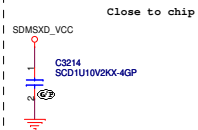
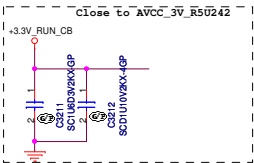
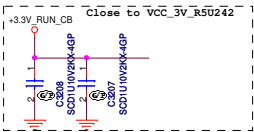
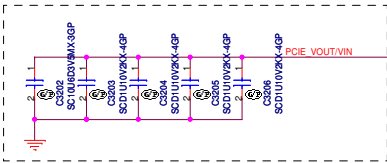
Title

**Reserve**

Size	Document Number	Rev
Custom	<b>Fonseca UMA</b>	<b>X02</b>

Date: Wednesday, March 10, 2010	Sheet 31 of 82
---------------------------------	----------------

SSID = 1394




Global Reset (GBRST#)  
Note:De-asserted before PERST# de-assertion

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<Core Design>



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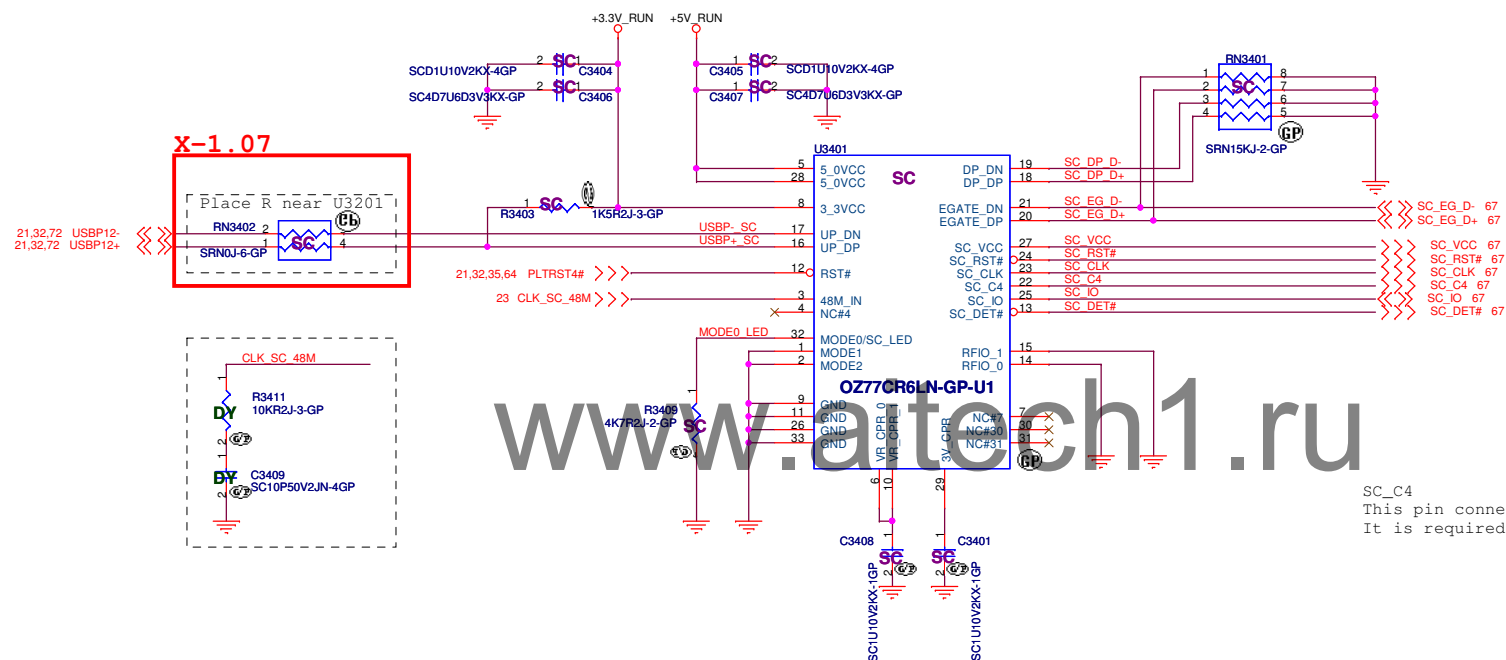
**Reserve**

Size	Document Number	Rev
Custom	<b>Fonseca UMA</b>	<b>X02</b>

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SSID = SmartCard

## SmartCard Chip

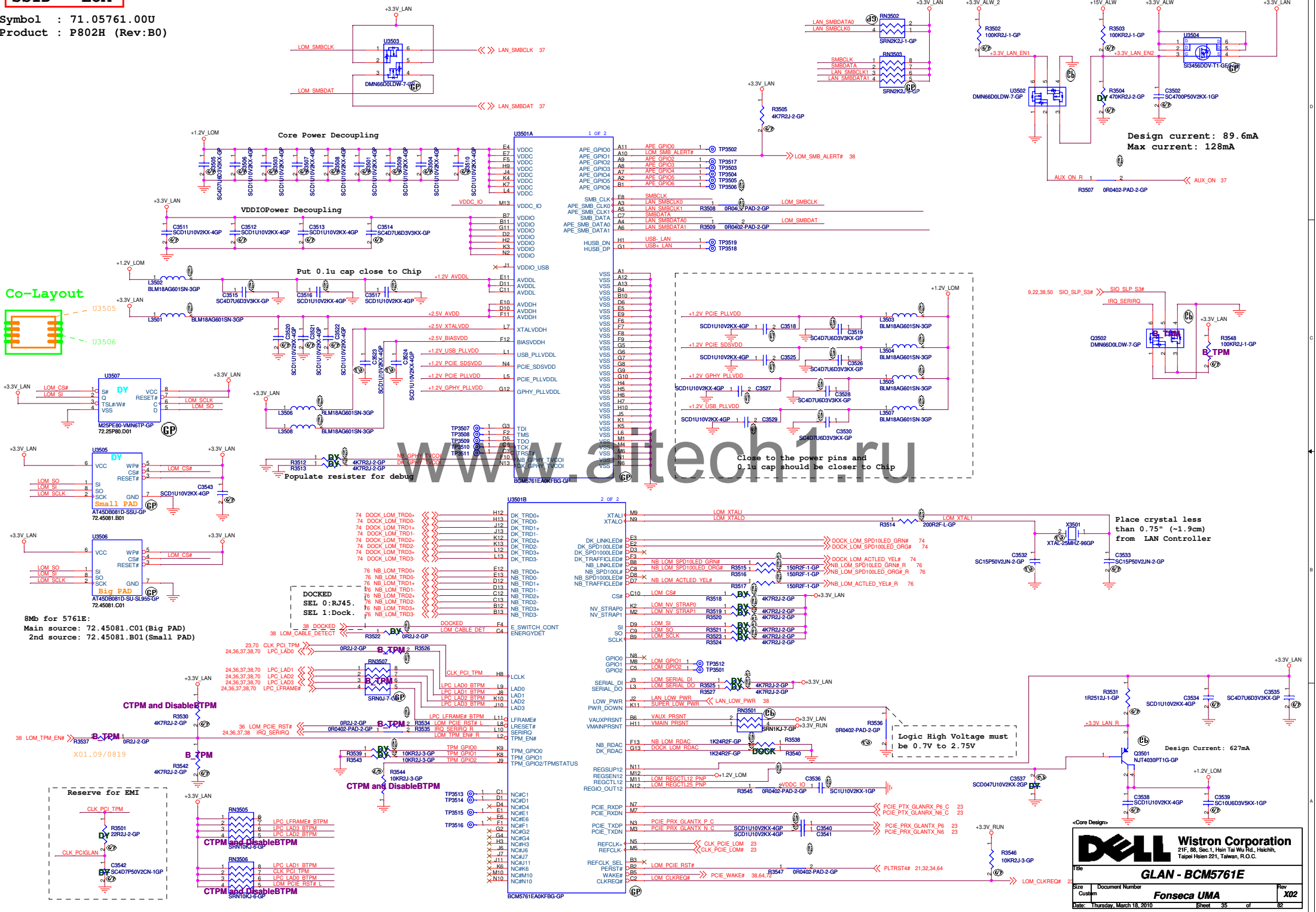


MODE0 / SC_LED	<p>This terminal is an output indicating Smart Card activity; capable to drive an external LED device. The SC_LED terminal drives a low logic level during Smart Card data read/write activity, and is capable to source 12mA of IOL current to drive an external LED circuit. When RST# is asserted, this terminal is sampled to select the downstream port configuration for DP_DP and DP_DN (Internal Port 1).</p> <p>When sampled low (4.7k), the downstream port device is removable.</p> <p>When sampled high, the downstream port is a non-removable device. Includes internal input pull-up resistor.</p>
MODE1	Test Pin. This terminal shall be externally connected to GND.
MODE2	Test Pin. This terminal shall be externally connected to GND.

RFIO_0	Contactless Smart Card Interface Signal 0 and 1. This signal provides detection and data communication with an external RF device.
RFIO_1	If contactless is disabled, then this terminal shall be pulled-down to GND through a pull-down resistor, or directly connected to GND.

<Core Design>

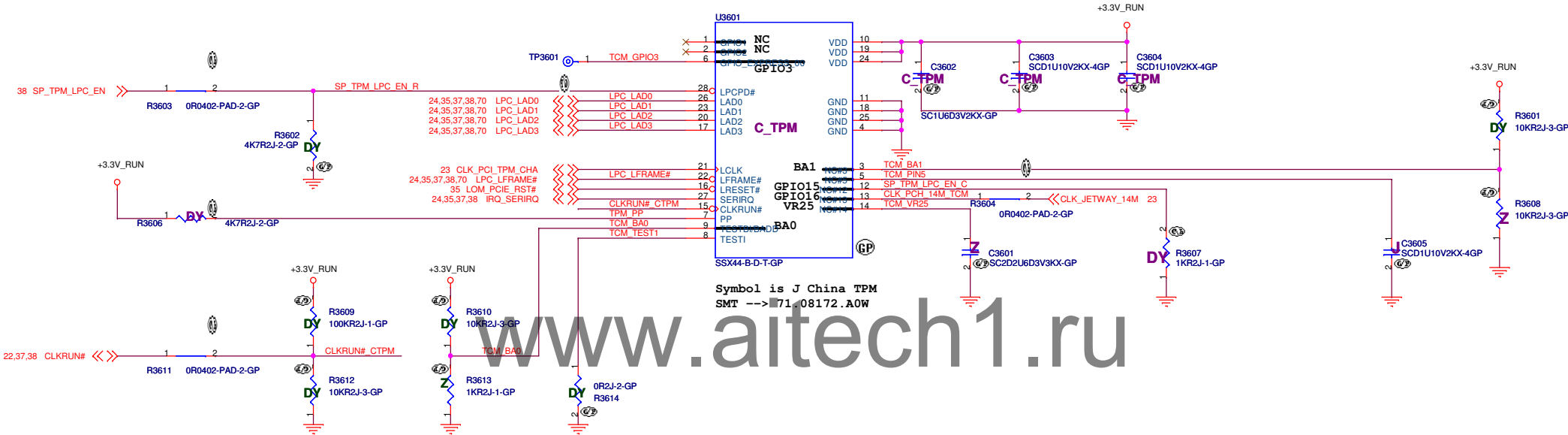
Symbol : 71.05761.00U  
Product : P802H (Rev:B0)



# SSID = TCM

Symbol : Jetway, but linked to ZTE  
 Product : 71.08172.00W (ZTE)

## China TPM Chip



Base Address	BA1 PIN3	BA0 PIN9
EE/EF	0	0
7E/7F	0	1
2E/2F	1	0
4E/4F	1	1

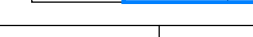
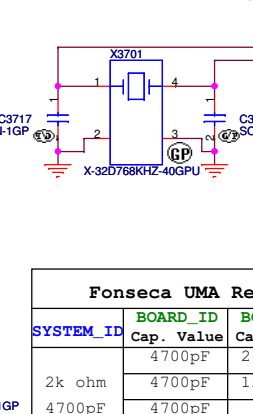
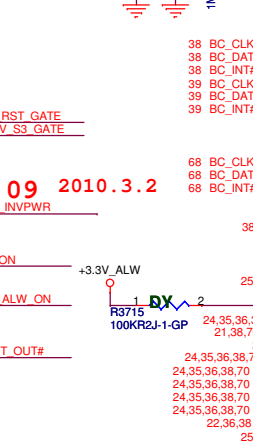
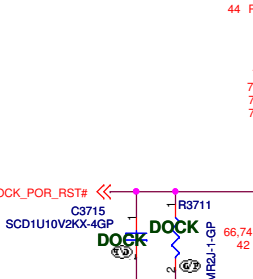
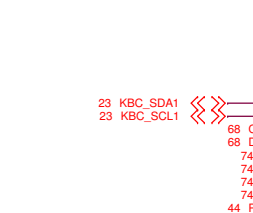
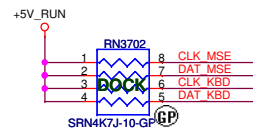
Default EE/EF as Any recommended

PIN12	FLASH	SRAM
1(default)	0	

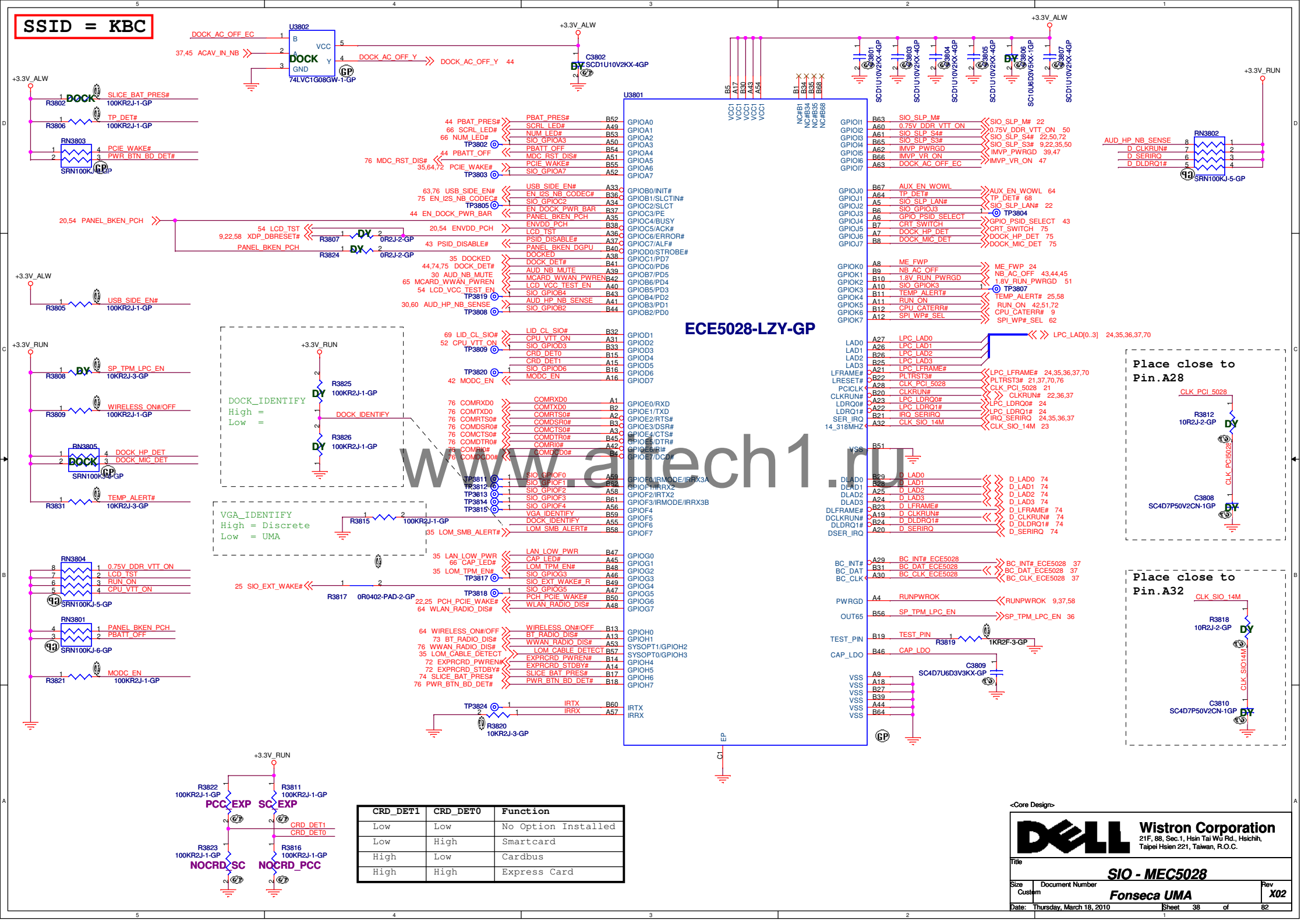
J has internal PU with PIN12.



SSID = KBC



SSID = KBC



ECE5028-LZY-GP

Place close to Pin. A28

Place close to Pin. A32

CRD_DET1	CRD_DET0	Function
Low	Low	No Option Installed
Low	High	Smartcard
High	Low	Cardbus
High	High	Express Card

<Core Design>

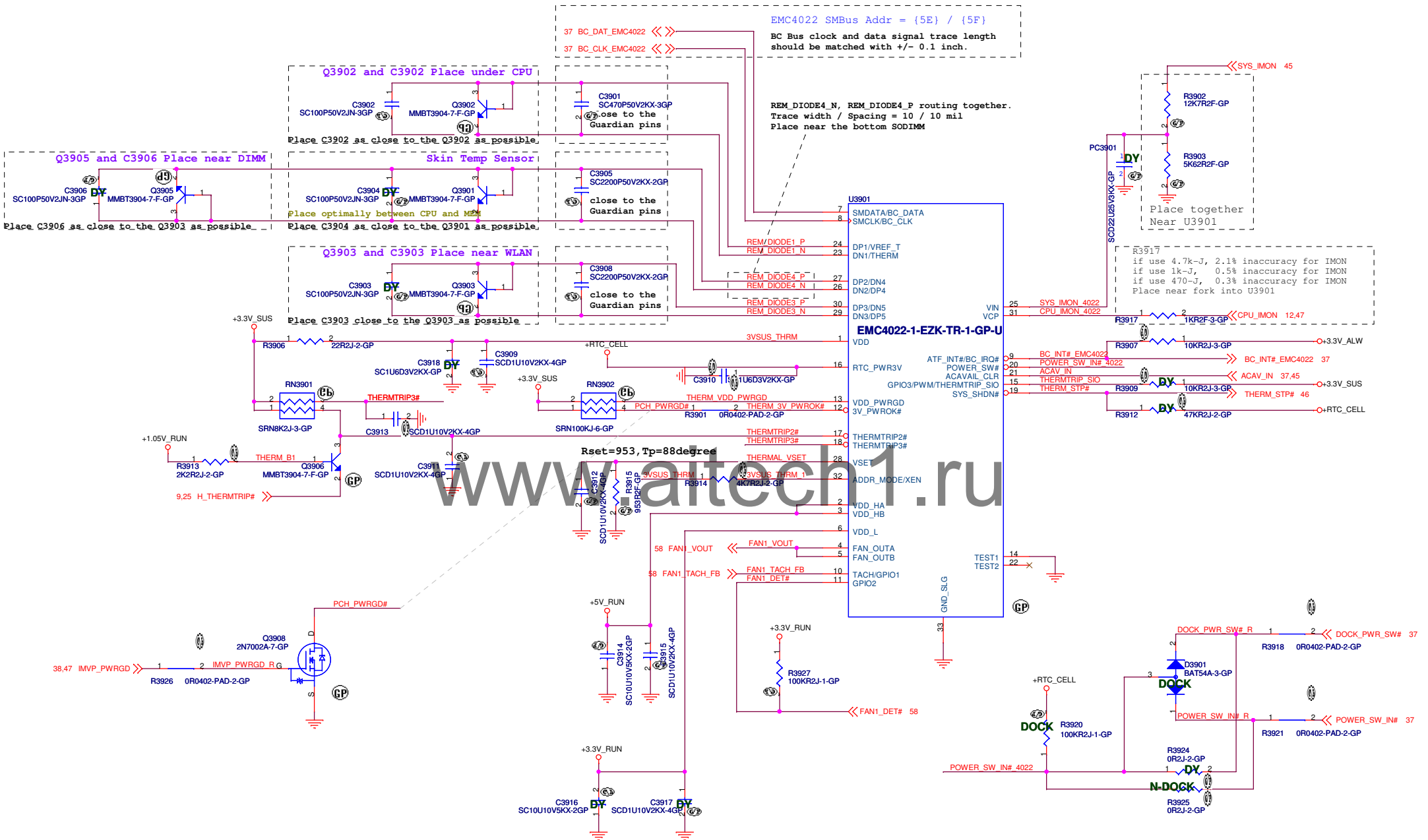
**DELL** Wistron Corporation  
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Taipei Hsien 221, Taiwan, R.O.C.

Title: **SIO - MEC5028**

Size: Custom Document Number: **Fonseca UMA** Rev: **X02**

Date: Thursday, March 18, 2010 Sheet: 38 of 82

## SSID = Thermal



### <Core Design>



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Title			
<b><i>Thermal Fan controller</i></b>			
Size	Document Number	Rev	
Custom	<b><i>Fonseca UMA</i></b>	<b><i>X02</i></b>	
Date: Thursday, March 18, 2010		Sheet 39	of 82



SSID = Reset.Suspend

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<Core Design>



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Taipei Hsien 221, Taiwan, R.O.C.

Title

Power On Logic

Size  
A3

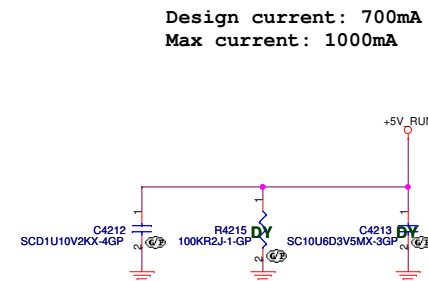
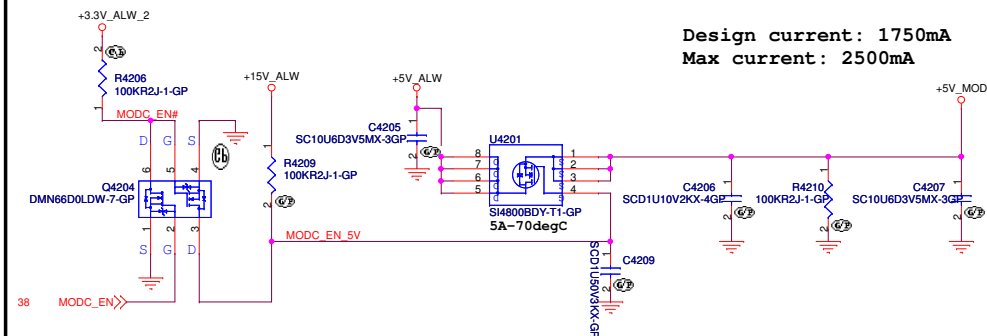
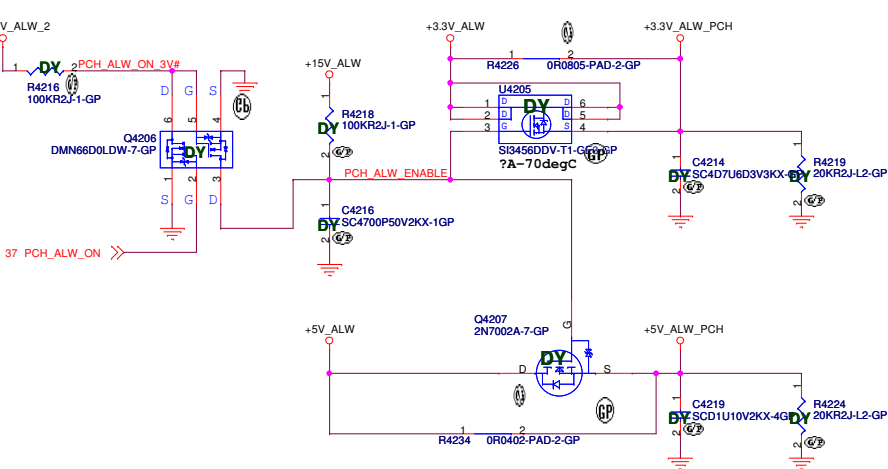
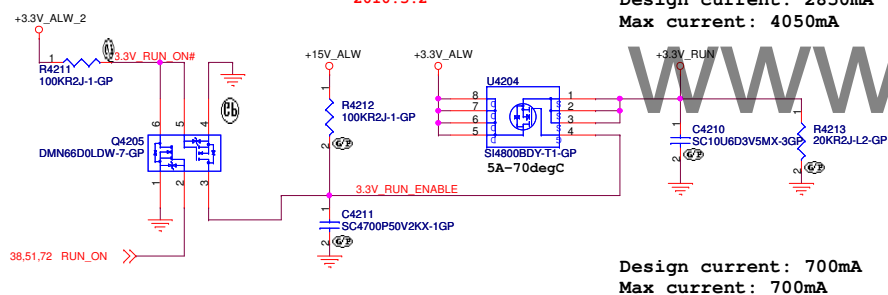
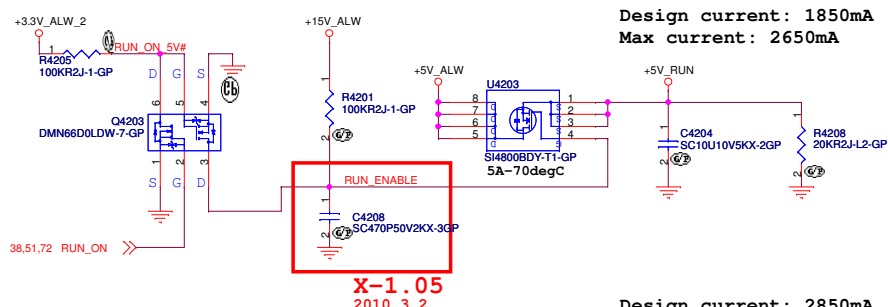
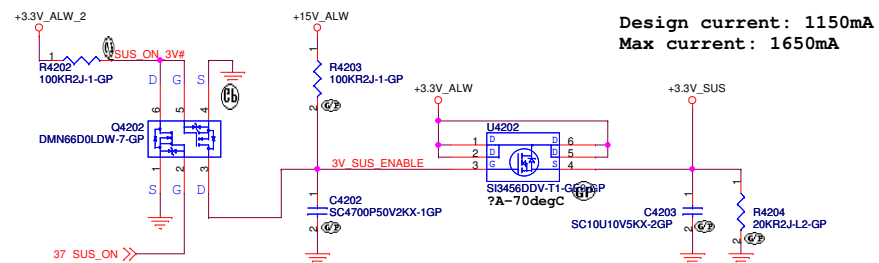
Document Number  
Fonseca UMA

Date: Wednesday, March 10, 2010

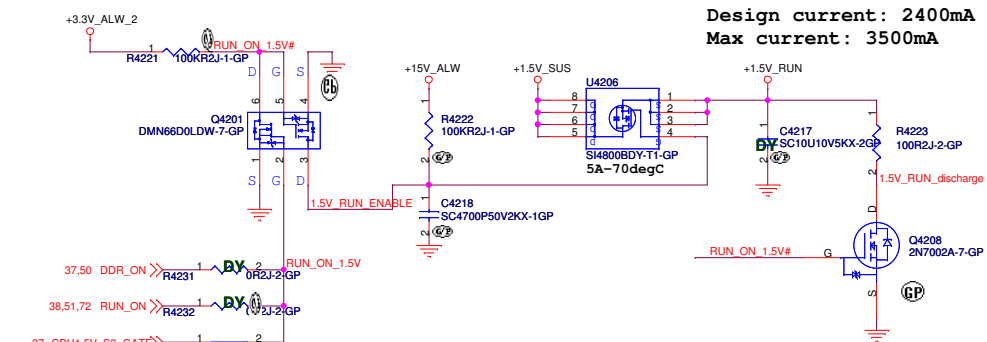
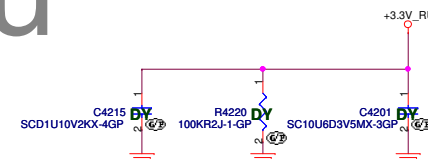
Rev  
X02

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# SSID = Reset . Suspend



place to HDD connector side



<Core Design>

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Title			Power Plane Enable
Size	Document Number	Rev	X02
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# SSID = PWR.Support

## Adapter In

### \*PIN NAME DIFFERENCES\*

PIN	MAXIM	INTERSIL	BQ24745
1	GND	NC	ICREF
3	REF	VREF	VREF
4	CCS	ICOMP	EAO
5	CCI	NC	EAI
6	CCV	VCOMP	FBO
7	DAC	NC	CE
8	IINP	ICM	VICM
11	VDD	VDDSMB	VDDSMB
14	BATSEL	NC	NC
15	FBSA	VFB	VFB
16	FBSB	NC	NC
17	CSIN	CSON	CSON
18	CSIP	CSOP	CSOP
20	DLO	LGATE	LGATE
21	LDO	VDDP	VDDP
23	LX	PHASE	PHASE
24	DHI	UGATE	UGSTE
25	BST	BOOT	BOOT
26	VCC	VCC	ICOUT

"NC" means no-connect

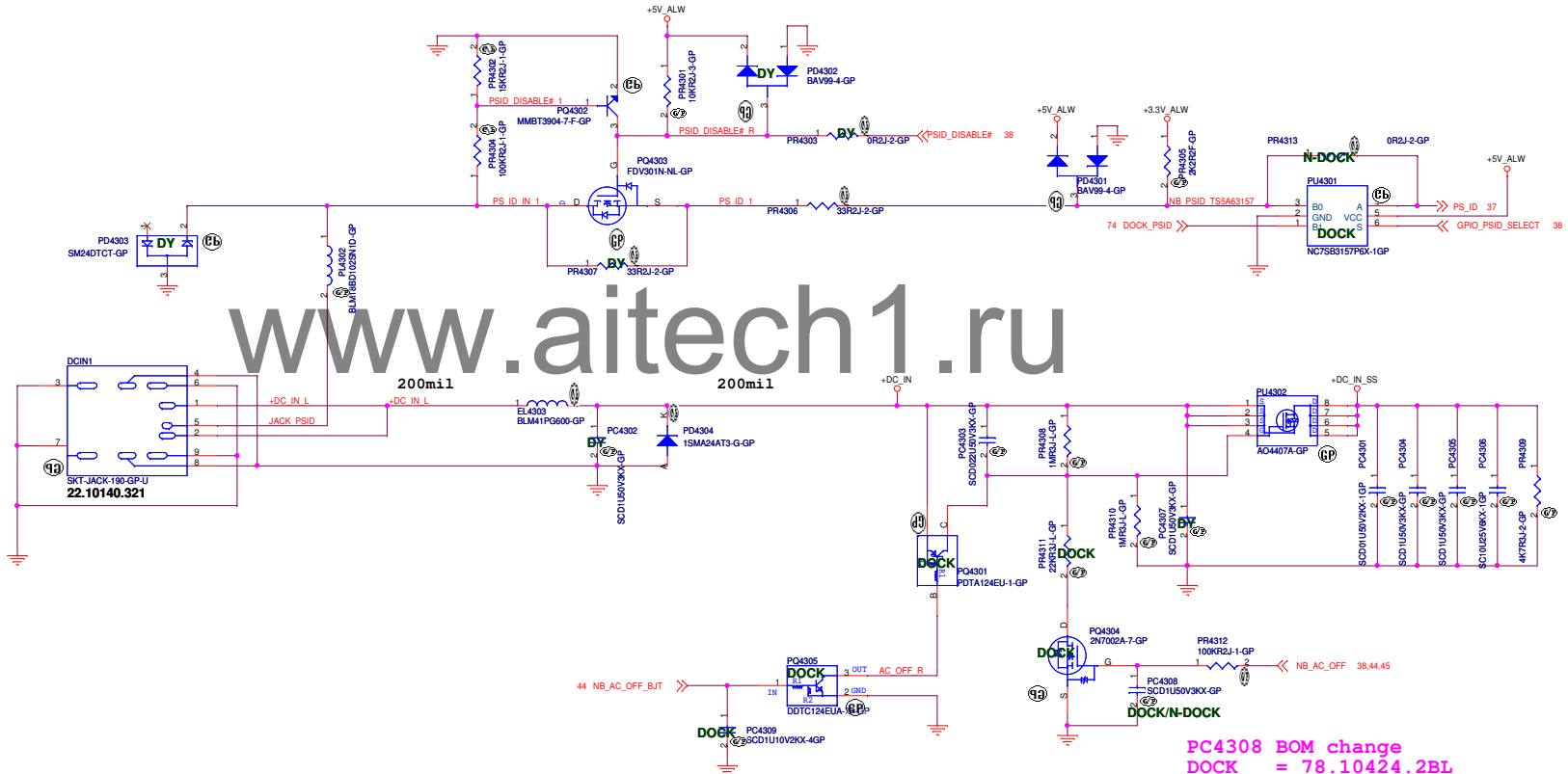
### DC IN CONN

PIN 3,4	DC_IN+
PIN 4,5	DC_IN-
PIN 1	ID
PIN 6,7,8,9	GND

### TABLE

#### MAXIM & INTERSIL BOM DIFFERENCES

REF DES	MAXIM	INTERSIL	TI
R411	8.45K 1%	DUMMY	DUMMY
C98	0.01uF	0.1uF	0.1uF
C459	0.1uF 10V	DUMMY	200P 10V
C5	1uF 10V	DUMMY	1uF 10V
R16	365K 1%	215K 1%	309K 1%
R434	0 5%	10 5%	0 5%
R414	0 5%	10 5%	0 5%
C473	DUMMY	0.22uF	0.1uF
C457	DUMMY	0.22uF	0.1uF
C442	0.01uF	DUMMY	DUMMY
C453	0.1uF 10V	DUMMY	DUMMY
C36	220pF 50V	DUMMY	DUMMY
D23	RB751V-40	DUMMY	RB751V-40
C58	3.3nF	DUMMY	DUMMY
R64	1 1%	0 5%	0 5%
R394	100 5%	0 5%	0 5%
R110	0 5%	8.45K 1%	8.45K 1%
R401	10K 5%	2.2K 5%	4.7K 5%
C441	0.01uF	0.01uF	DUMMY
C449	0.01uF	0.01uF	DUMMY
R397	1K 5%	DUMMY	DUMMY
Q41	ISS355	DUMMY	DUMMY
C16	1uF 10V	1uF 10V	DUMMY
R30	33 1%	33 1%	DUMMY
R408	DUMMY	DUMMY	0 5%
R400	DUMMY	DUMMY	200K 5%
R403	DUMMY	DUMMY	7.5K 5%
C450	DUMMY	DUMMY	51P 10V
C444	DUMMY	DUMMY	2000P 10V
C448	DUMMY	DUMMY	130P 10V
C446	DUMMY	DUMMY	0.1uF
C483	DUMMY	DUMMY	0.1uF
R438	10K 1%	10K 1%	10K 1%
R412	DUMMY	DUMMY	10K 5%
R440	15.8K 1%	15.8K 1%	DUMMY
R407	DUMMY	DUMMY	10K 5%
R9	0 5%	10 5%	0 5%
C482	DUMMY	DUMMY	DUMMY
C12	DUMMY	DUMMY	DUMMY
R435	0 5%	10 5%	0 5%



PC4308 BOM change  
DOCK = 78.10424.2BL  
N-DOCK = 63.00000.00L

MAX 8731A/ISL88731

Adapter (W)	Trip Current (A)	R416	R502	R501	R504
65	3.17	57.6K	13.0K	105	24.9K
90	4.43	51.1K	17.8K	348	33.2K

\*R504 is populated if ADAPT\_TRIP\_SEL is used to program for the next lower adapter.

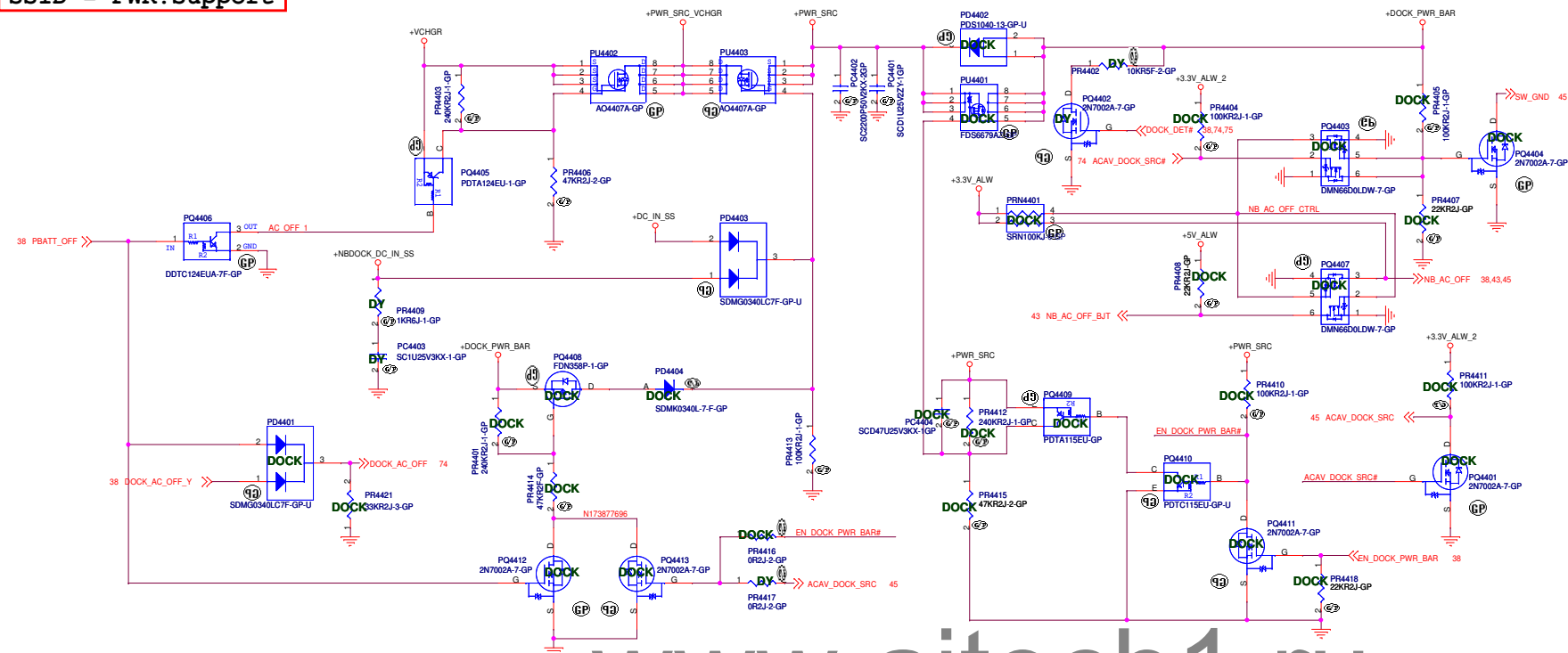
BQ247451

Adapter (W)	Trip Current (A)	R416	R502	R501	R504
65	3.17	57.6K	12.4K	205	24.3K
90	4.43	51.1K	16.9K	499	32.4K

\*R504 is populated if ADAPT\_TRIP\_SEL is used to program for the next lower adapter.

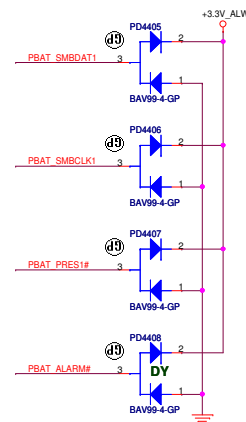
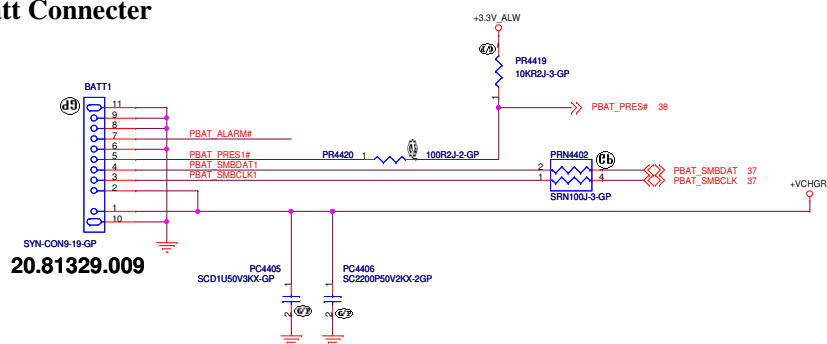


## SSID = PWR.Support



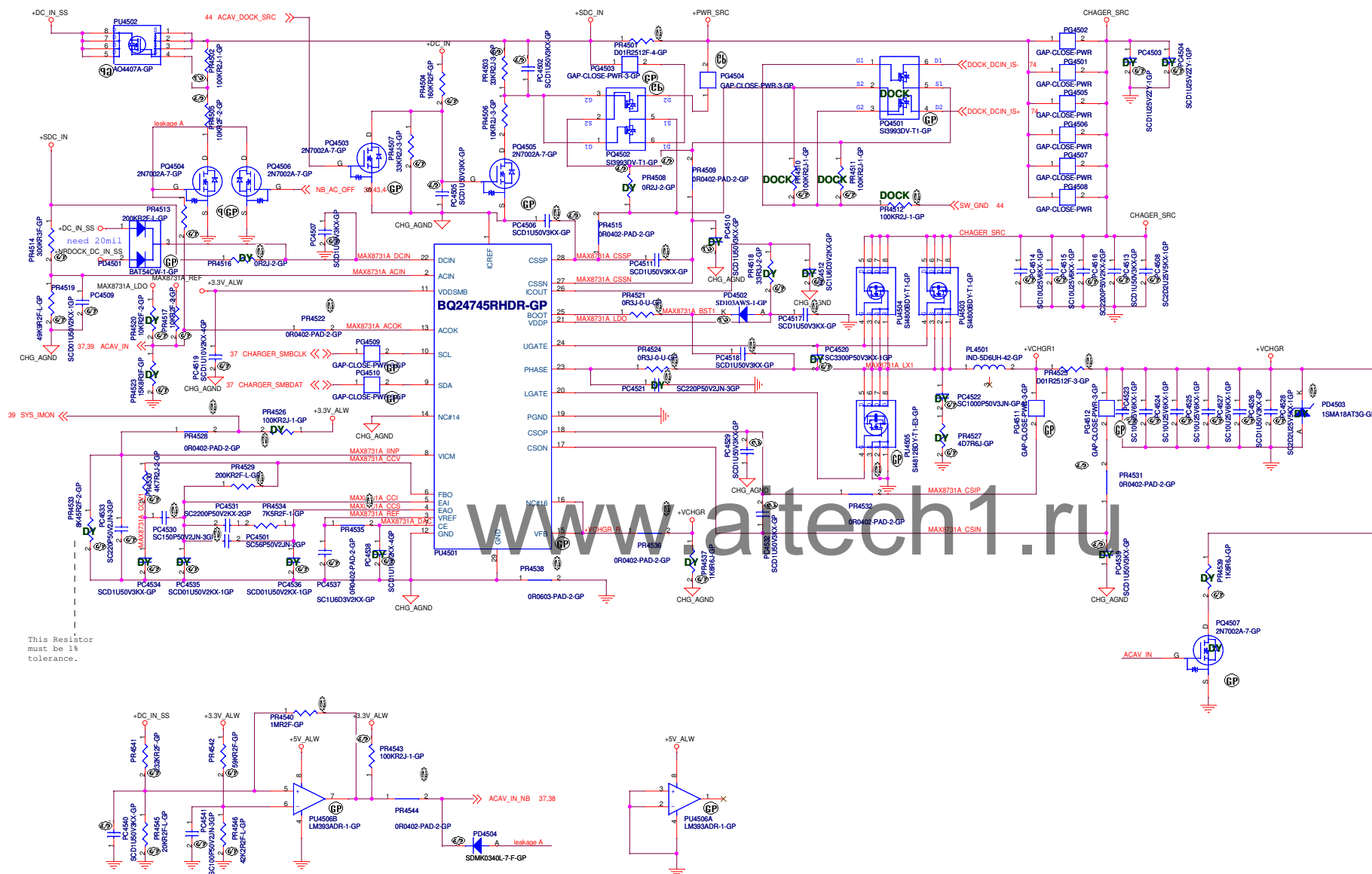
**SSID = RBATT**

## Batt Connector

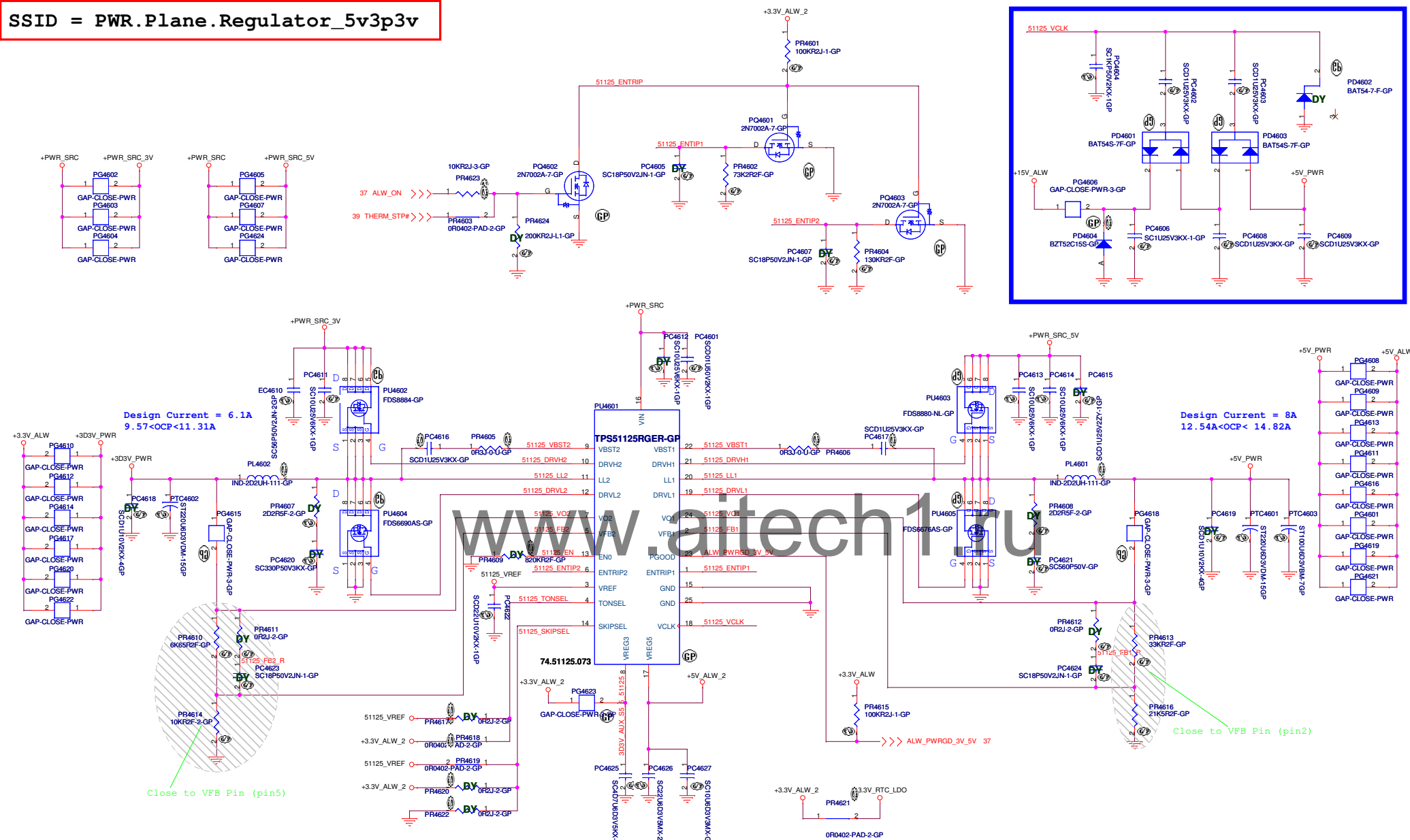




## SSID = Charger



```
SSID = PWR.Plane.Regulator_5v3p3v
```



```
I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: FDVE0630-1R5M-P3 TOKO 10.6 mohm Isat =10.7Arms 68.1R510.10Y
O/P cap: 220U 6.3V PSLV0P27 T0K0 (25 25mOhm 2.236Arms NEC_TOKIN/77.C2271.00L
O/P cap: 100U 6.3V PTE100MAZB 35mOhm 1.4Arms SANYO/77.21071.07L
H/S: FDS58884 SO-8 / 23mohm/30mOhm@4.5Vgs/ 84.08884.037
L/S: FDS6690A5 SO-8 / 12mohm/15mOhm@4.5Vgs/ 84.06690.P37
```

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L  
Inductor: FDU0630-22M2M-P3 TOKO 14mohm Isat = 9.4Arms 68.2R21B.10A  
O/P cap: 220U 6.3V PSLV0J227M(25) 25mOhm 2.236Arms NEC\_TOKIN/77.C2271.00L  
H/S: FDS8889AS SO-8 23mohm/30mOhm@4.5Vgs/ 84.08884.037  
L/S: FDS6690AS SO-8 12mohm/15mOhm@4.5Vgs/ 84.06690.E37

SKIPSEL	VREG3 or VREG5	VREF (2V)	GND
Operating Mode	OOA Auto Skip	Auto Skip	PWM only

EN0	Open	820kΩ to GND	GND
Operating Mode	enable both LDOs, VCLK on and ready to turn on switcher channels	enable both LDOs, VCLK off and ready to turn on switcher channels	disable all circuit

TONSEL	CH1	CH2
GND	200kHz	265kHz
VREF	245kHz	305kHz
VREG3	300kHz	375kHz
VREG5	365kHz	460kHz

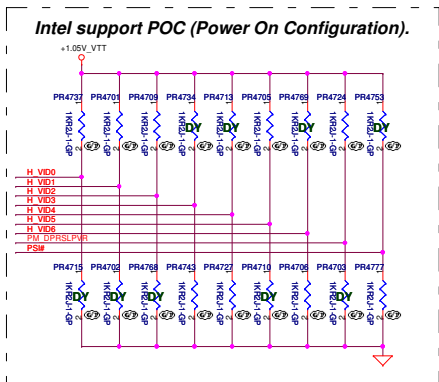
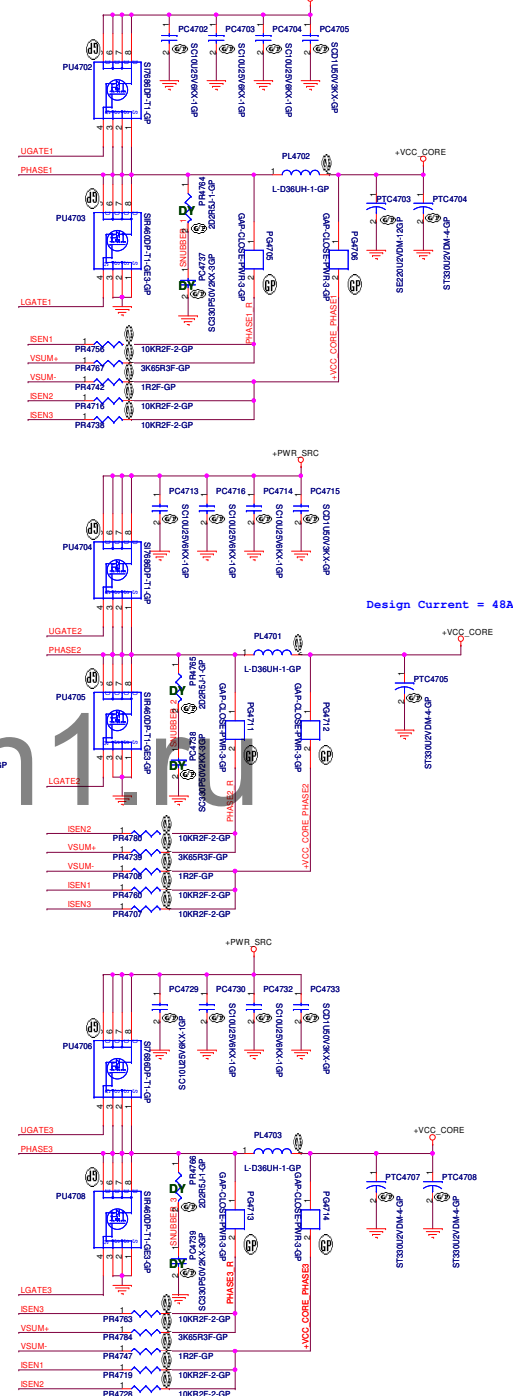
&lt;Core Design&gt;



Title **DCDC 5V/3D3V (TPS51125)**

Size	Document Number	<b>Fonseca UMA</b>
Custom		


Date: Wednesday, March 17, 2010 Sheet 46 of 82



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Title


Reserve

Size A3	Document Number Fonseca UMA	Rev X02
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SSID = PWR.Plane.Regulator\_1p05v

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<Core Design>



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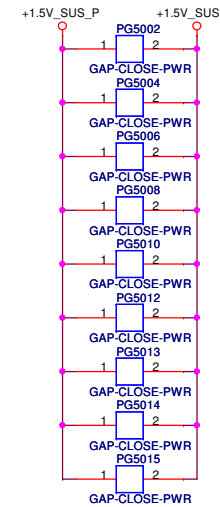
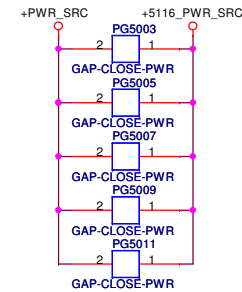
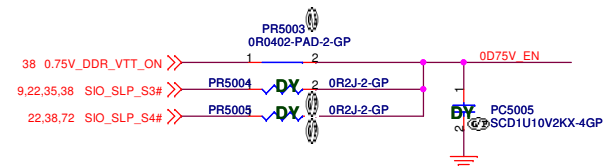
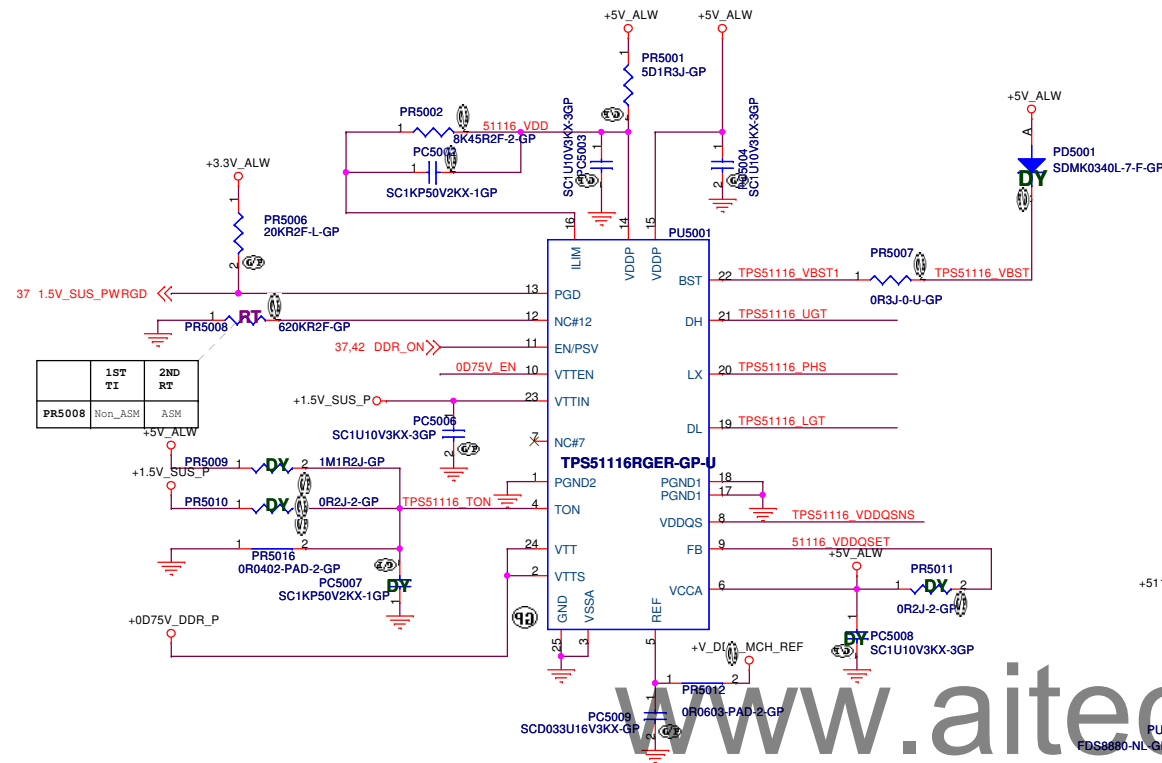
Title

**DC to DC 1.05V**

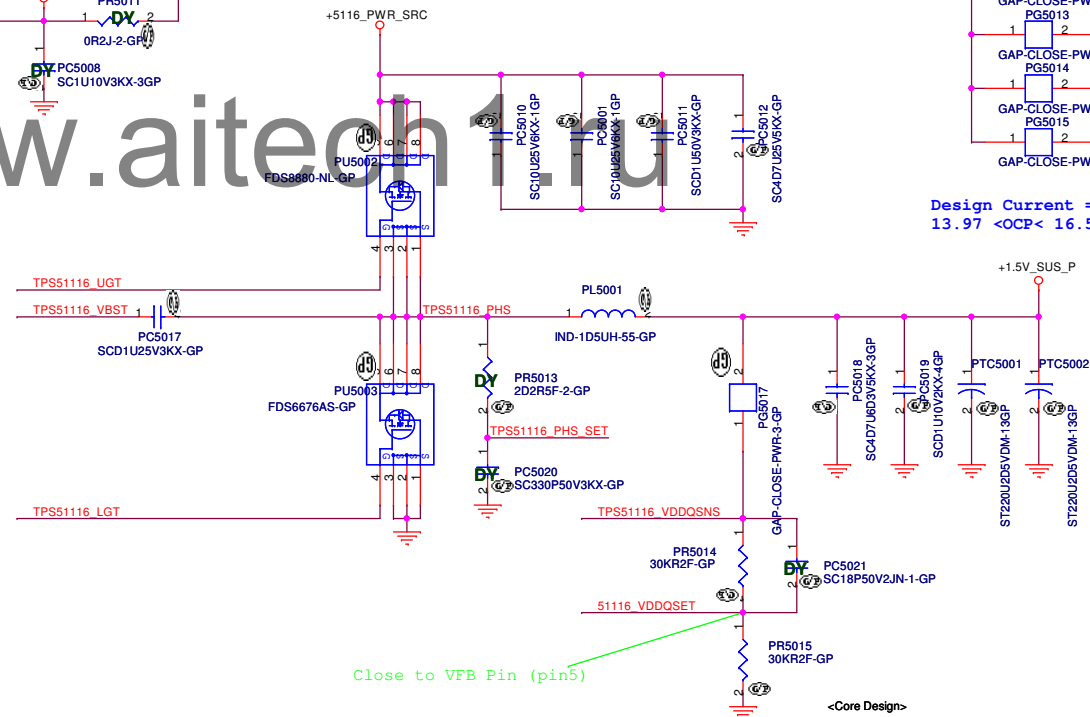
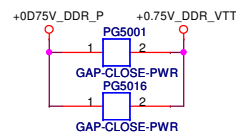
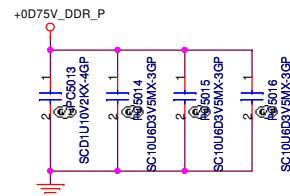
Size A3	Document Number <b>Fonseca UMA</b>	Rev <b>X02</b>
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SSID = PWR.Plane.Regulator\_1p5v0p75v



Design Current = 8.9A  
13.97 <OCV< 16.51A



State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

VDDQSET	VDDQ (V)	VTTREF and VTT	NOTE
GND	2.5	VVDDQSNS/2	DDR
V5IN	1.8	VVDDQSNS/2	DDR2
FB Resistors	Adjustable	VVDDQSNS/2	1.5 V < VVDDQ < 3 V

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L  
Inductor: FDU1040-1R5M=P3 TOKO DCR:3.86 mohm Isat =19.7Arms 68.1R510.10Q  
O/P cap: TLP5LV0G227M(25)12RE 25mOhm 2.5Arms NEC\_TOKIN/ 77.C2271.07L  
H/S: FDS8880 SO-8/9.6mohm/ 12mOhm@4.5Vgs/ 84.08880.037  
L/S: FDS8672S SO-8/ 5.3mohm/7.0mohm@4.5Vgs/ 84.08672.A37  
Switching freq-->400KHz

Close to VFB Pin (pin5)

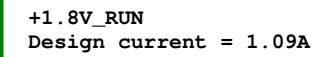
<Core Design>

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File **DC to DC 1.5V / 0.75V**

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### ***LDO for +1.8V\_RUN***



SSID = PWR.Plane.Regulator\_1p05v

## TPS51218 for +1.05V\_VTT

Frequency setting  
420K -->290KHz  
200K -->340KHz  
100K -->380KHz  
39K -->430KHz

$$V_{out} = 0.704V * (R1 + R2) / R2$$

Max. Current = 18A  
Design Current = 18A  
19.8<OCP<23.4A

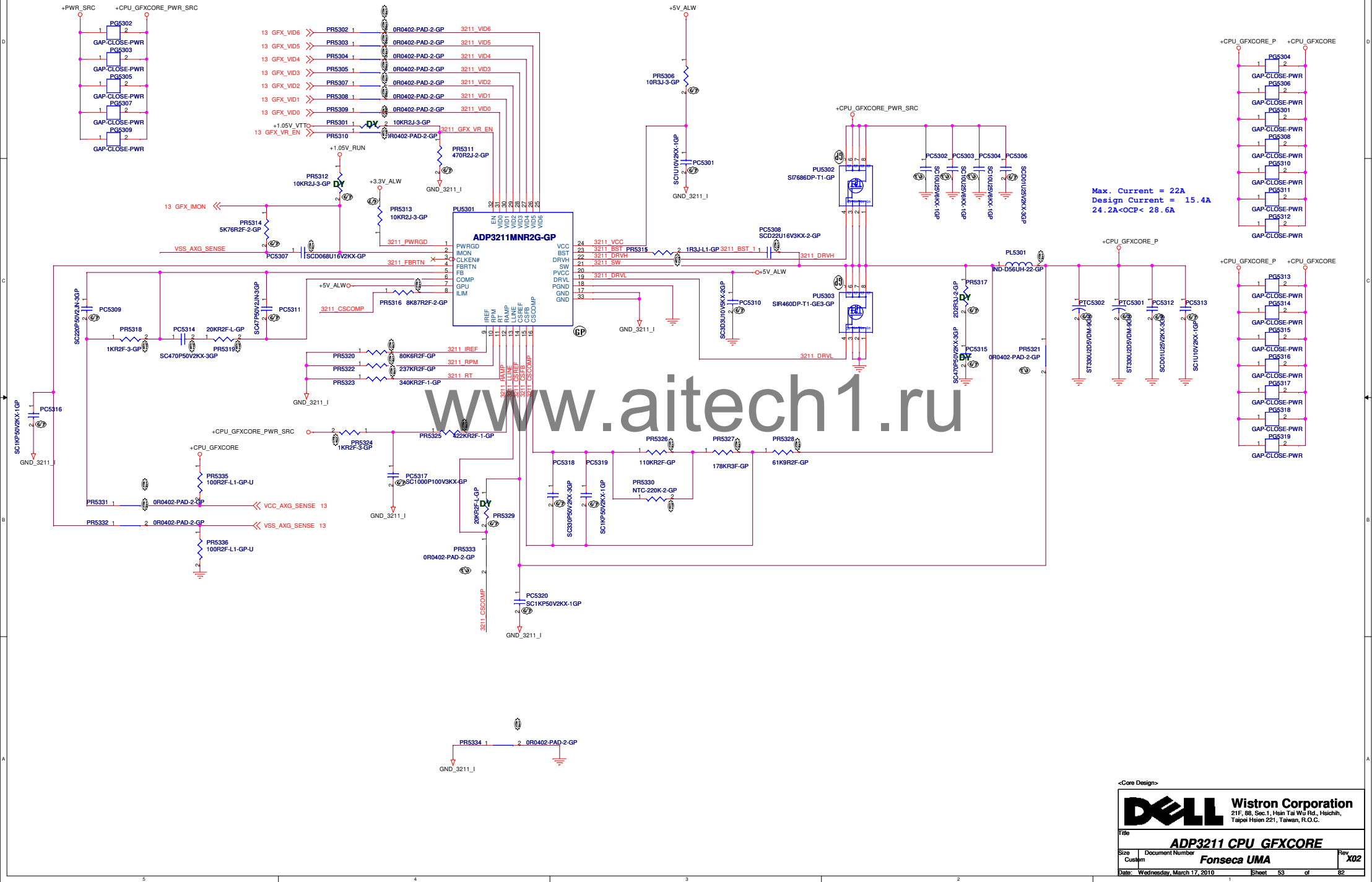
<Core Design>

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Title **DC to DC +1.05V\_VTT**  
Size Document Number **Fonseca UMA** Rev **X02**  
Date: Wednesday, March 17, 2010 Sheet 52 of 82



SSID = CPU.GFX.Regulator



<Core Design>

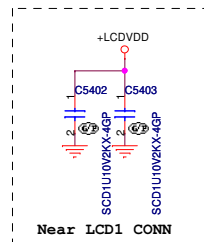
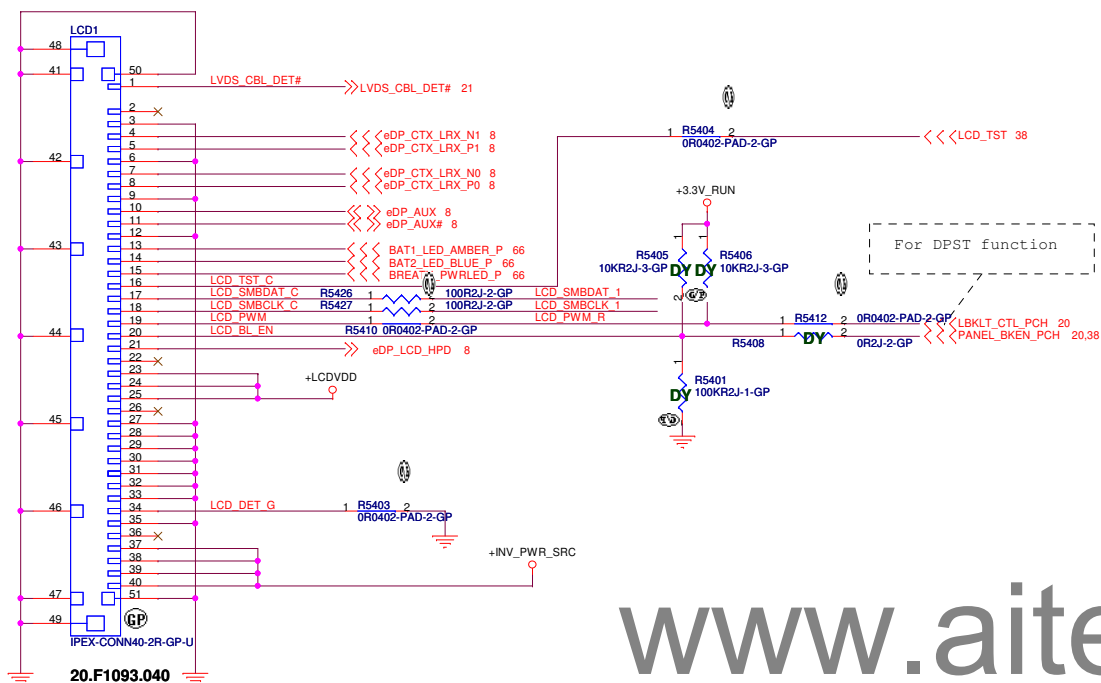
<b>DELL</b>		<b>Wistron Corporation</b>	
21F, 88, Sec.1, Hsin Tai Wu Rd., Heichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title			
<b>ADP3211 CPU GFXCORE</b>			
Size	Document Number	Rev	
Custom	<b>Fonseca UMA</b>		<b>X02</b>
Date:	Wednesday, March 17, 2010	Sheet	53 of 82

SSID = VIDEO

LED Location from left to right

---

**BATTERY**



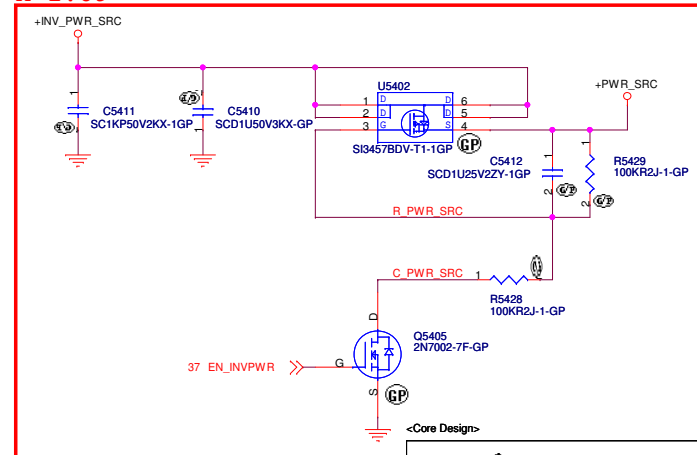
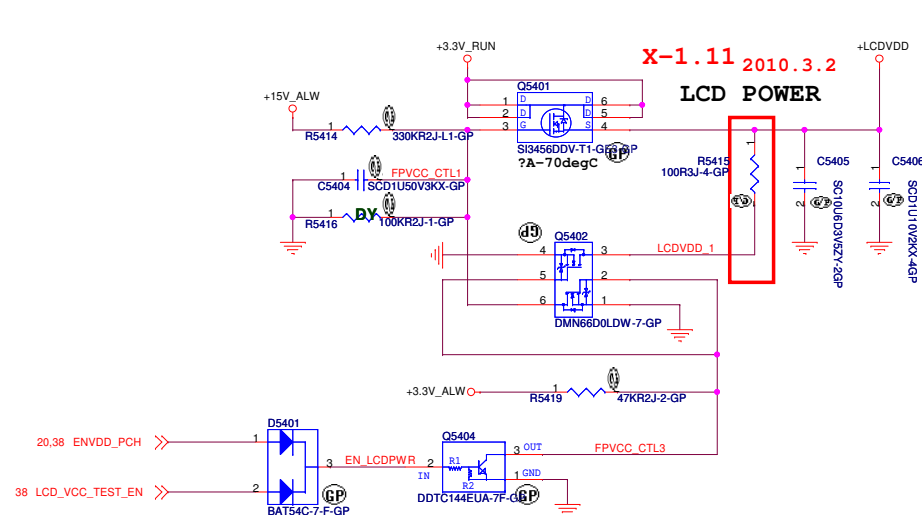
www.aitech1.ru

SSID = VIDEO

SSID = Inverter

## LED BACKLIGHT CONVERTER POWER

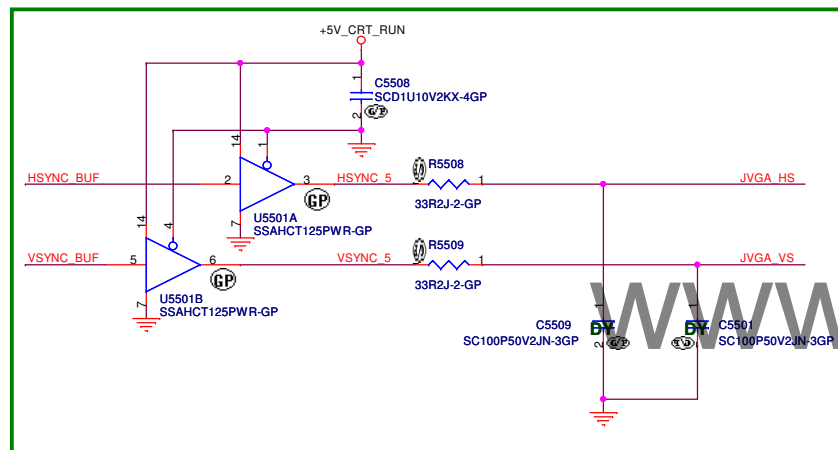
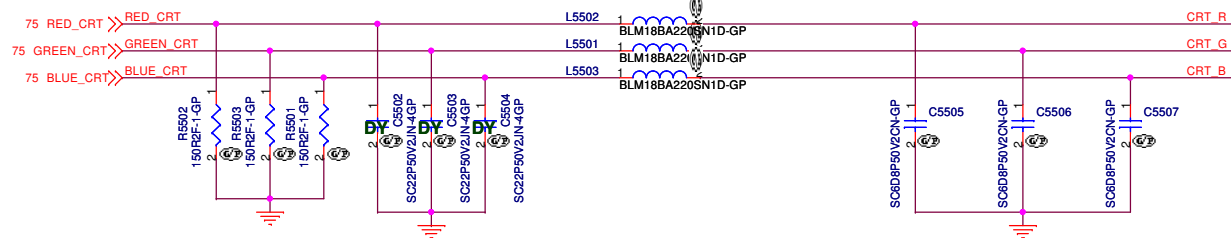
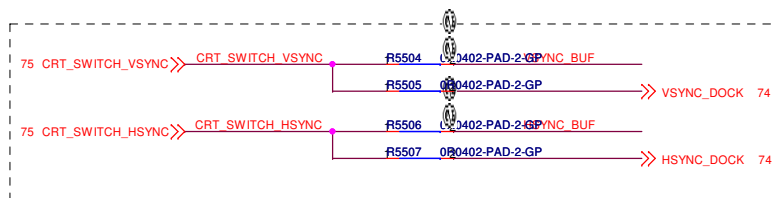
**X-1.09 2010.3.2**



**DELL** **Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

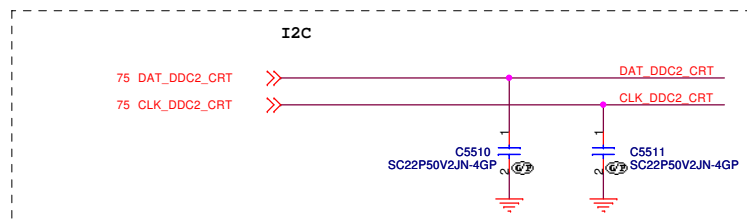
Title			
<b>LCD</b>			
Size	Document Number	Rev	
Custom	<b>Fonseca UMA</b>	X0	
Date: Wednesday, March 17, 2010		Sheet 54 of	82

SSID = VIDEO

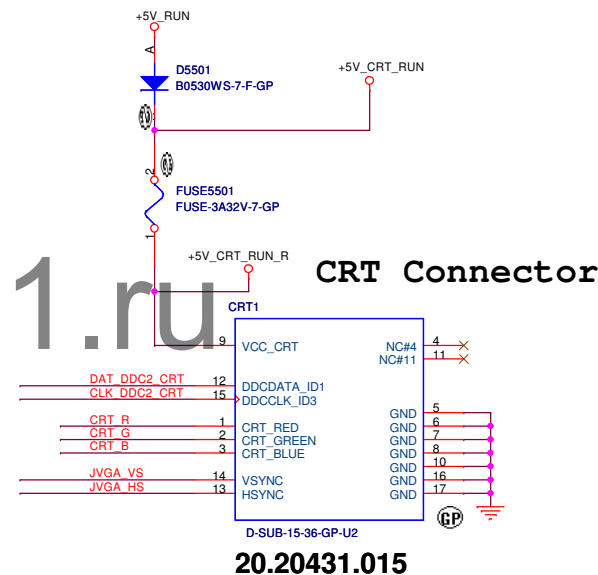


Layout Note:

- \*Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN.
- \* RGB signal will hit 75 Ohm first, then pi-filter, finally CRT CONN.



MAX4885E has internal ESD protection and internal level shift



X-1.20 2010.3.10

AFTP5501 1 CRT\_R

<Core Design>



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Title

CRT

Size  
A3

Document Number

Fonseca UMA

Rev  
X02


Date: Thursday, March 18, 2010

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<Core Design>



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Title

Size  
A3

Document Number  
**Fonseca UMA**


Rev  
**X02**

Date: Wednesday, March 10, 2010Sheet 56 of 82

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<Core Design>



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Taipei Hsien 221, Taiwan, R.O.C.

Title

Size  
A3

Document Number  
**Fonseca UMA**

Date: Wednesday, March 10, 2010

Rev  
**X02**

Sheet 57 of 82

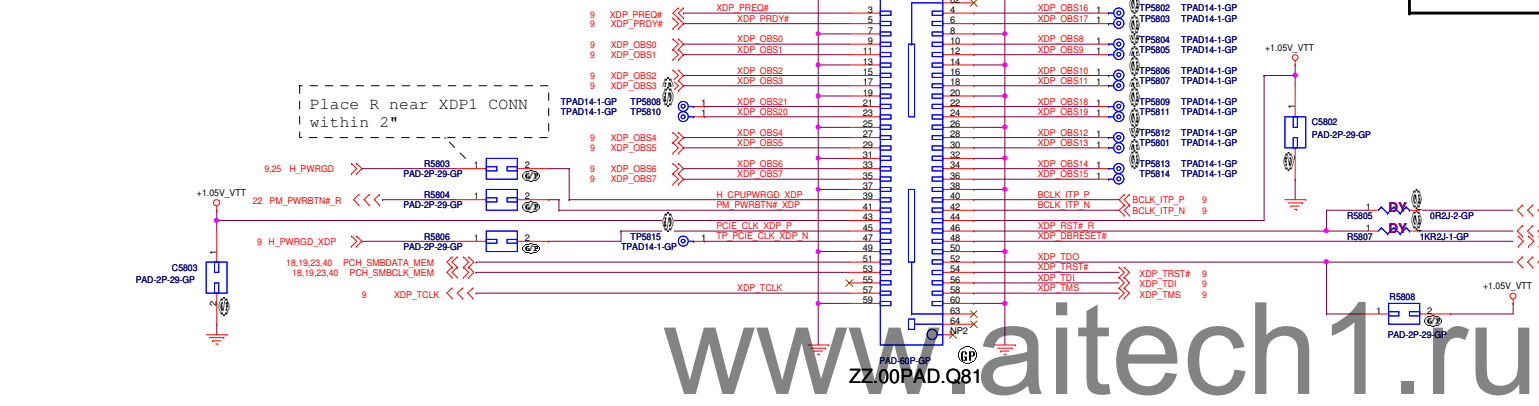
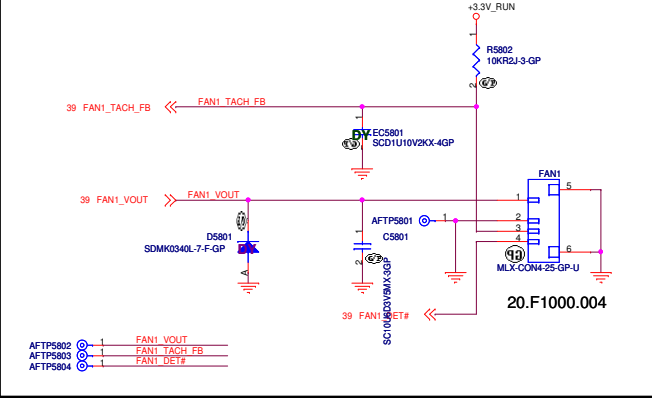
SSID = CPU X-1.02 2010.3.2

LOCATION	POP P/N	DY P/N
XDP1, XDP2	20.F0971.060	ZZ.00PAD.Q81
C5802	78.10421.2FL	ZZ.00PAD.Q71
C5803	78.10421.2FL	ZZ.00PAD.Q71
R5803	63.10234.1DL	ZZ.00PAD.Q71
R5804	63.R0034.1DL	ZZ.00PAD.Q71
R5806	63.R0034.1DL	ZZ.00PAD.Q71
R5808	63.51034.1DL	ZZ.00PAD.Q71

X-1.12 2010.3.10

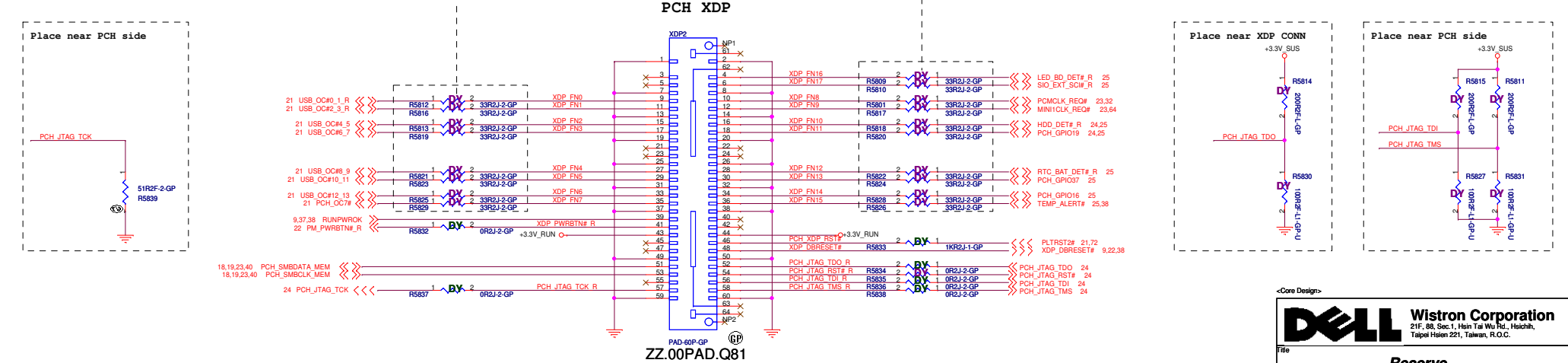
LOCATION	POP P/N	DY P/N
TP5801~TP5815	ZZ.PAD14.001	ZZ.00PAD.Q91

SSID = Thermal

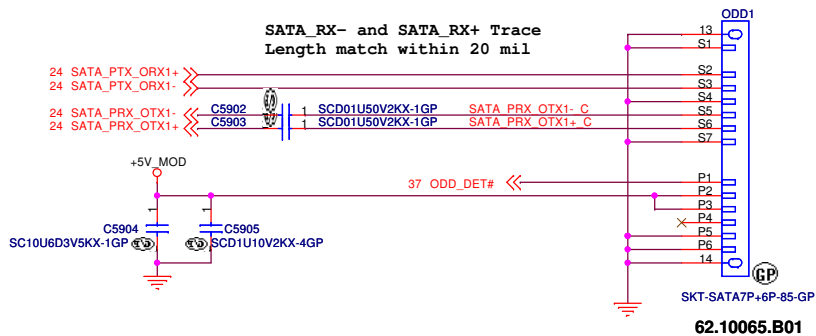


SSID = PCH

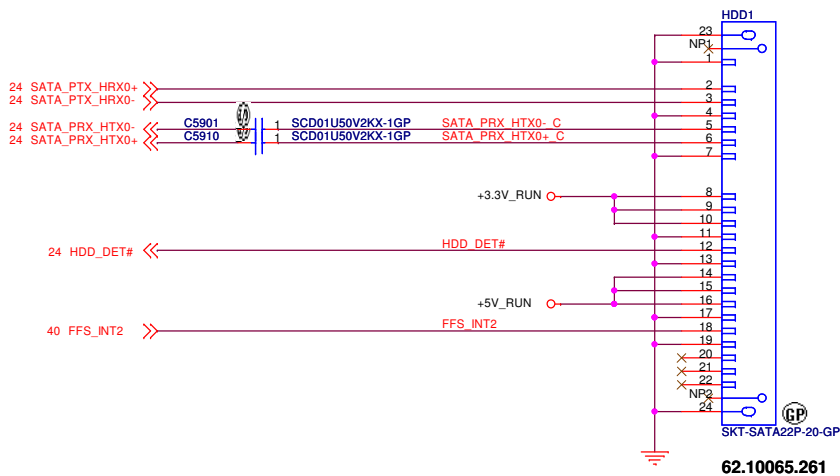
A 33 ohm series resistor should be placed within 1 inch (or 25.4 mm) of the PCH to source terminate the interface.



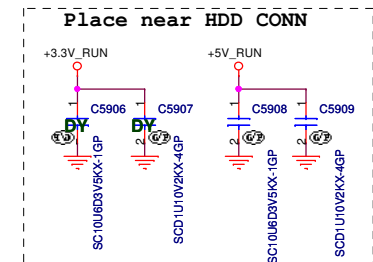
# SSID = SATA SATA ODD Connector



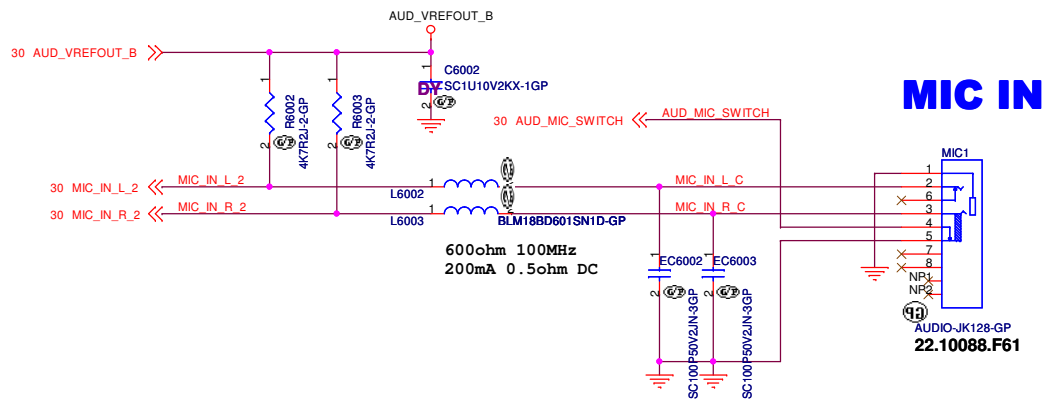
# SSID = SATA SATA HDD Connector



SATA HDD Interface comment  
\*\*\*\*\*  
--- GND  
RX+  
RX-  
TX-  
TX+  
--- GND  
\*\*\*\*\*  
----- 3.3V  
----- 3.3V  
----- 3.3V  
--- GND  
--- GND / Dell Detected Pin  
--- GND  
----- 5V  
----- 5V  
----- 5V  
--- GND  
(Dell: FFS\_INT for supported HDD)  
--- GND  
----- 12V (No support)  
----- 12V (No support)  
----- 12V (No support)  
\*\*\*\*\*

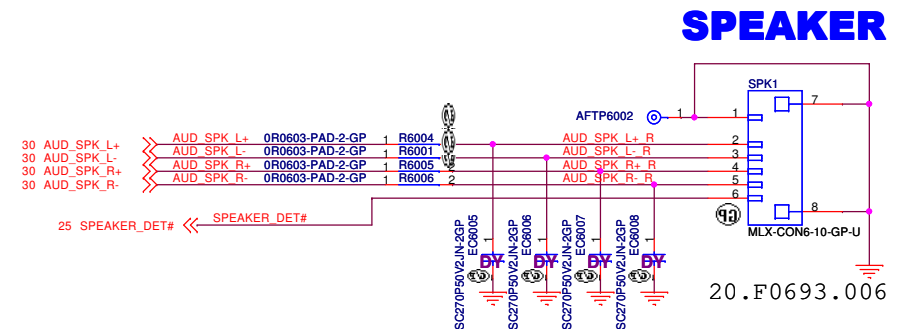


SSID = AUDIO



MIC IN

SSID = AUDIO

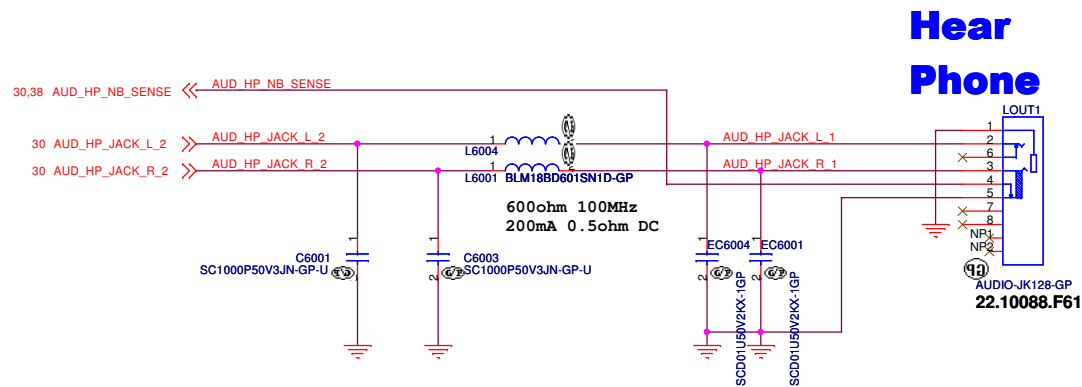


SPEAKER

AFTP6003 AUD SPK L+ R  
AFTP6004 AUD SPK L- R  
AFTP6005 AUD SPK R+ R  
AFTP6001 AUD SPK R- R  
AFTP6006 SPEAKER\_DET#

SSID = AUDIO

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Hear  
Phone

<Core Design>

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Title  
**Audio Jack / Speaker Connector**  
Size A3 Document Number  
**Fonseca UMA** Rev  
**X02**  
Date: Thursday, March 18, 2010 Sheet 60 of 82



SSID = LOM

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<Core Design>



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Taipei Hsien 221, Taiwan, R.O.C.

Title

Size  
C

Document Number  
**Fonseca UMA**

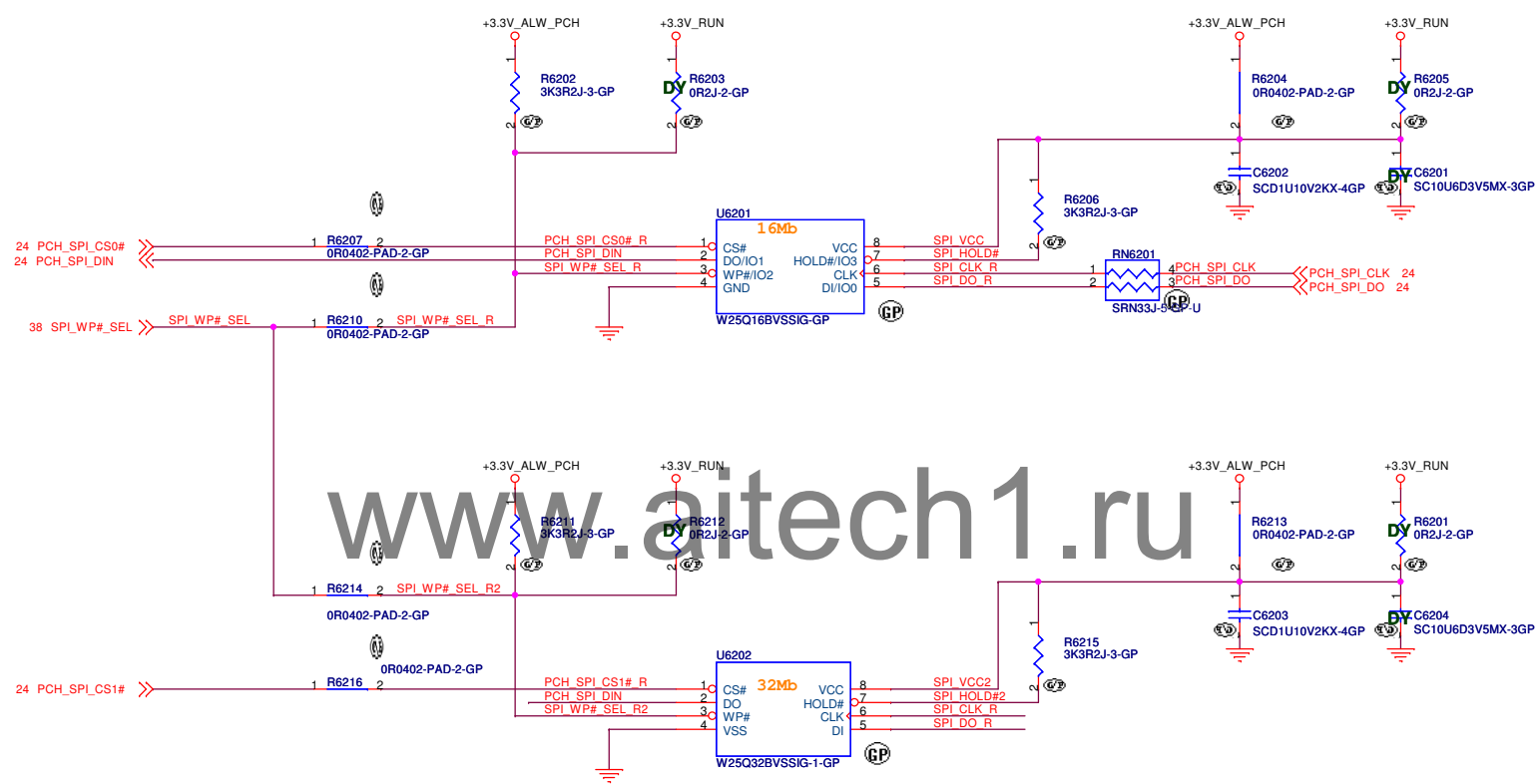
Rev  
**X02**

Date: **Wednesday, March 10, 2010**

Sheet **61** of **82**

**Reserve**

SSID = Flash.ROM

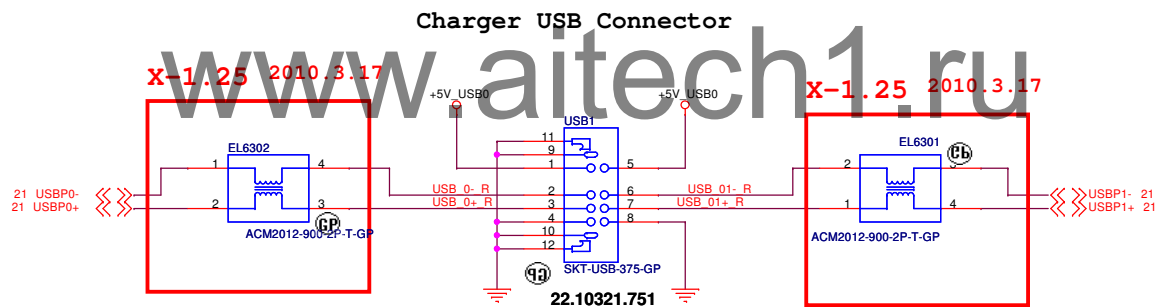
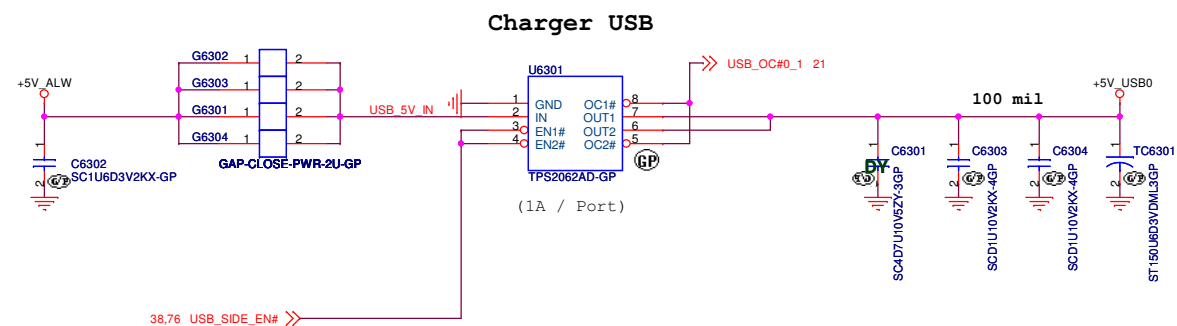


- #1 source: 72.25Q16.001 (2MB, Winbond)  
#2 source: 72.25165.B01 (2MB, MXIC)  
#3 source: 72.02516.A01 (2MB, Numonyx)
- #1 source: 72.25Q32.A01 (4MB, Winbond)  
#2 source: 72.25325.A01 (4MB, MXIC)  
#3 source: 72.25P32.B01 (4MB, Numonyx)

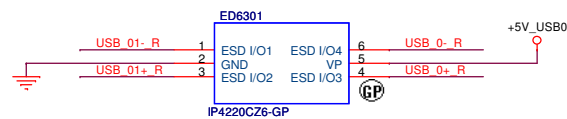
Pin.2  
From Intel checklist,  
SPI\_CS#/CS1#  
No series resistor required  
if routing length is 1.5"-6.5"  
(with 1 or 2 SPI device)

Pin.6  
Intel checklist  
No series resistor required if routing length is 1.5"-6.5"  
(with 1 or 2 SPI device)

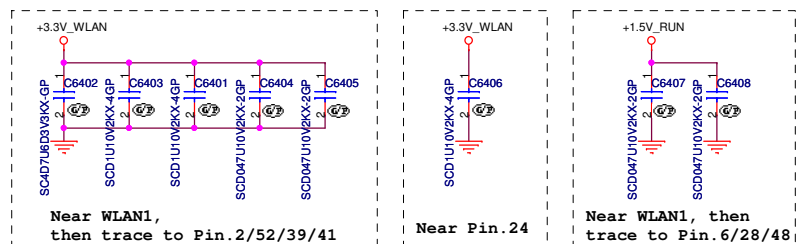
SSID = USB



S	OE#	Function
X	H	Disconnect
L	L	D=1D
H	L	D=2D



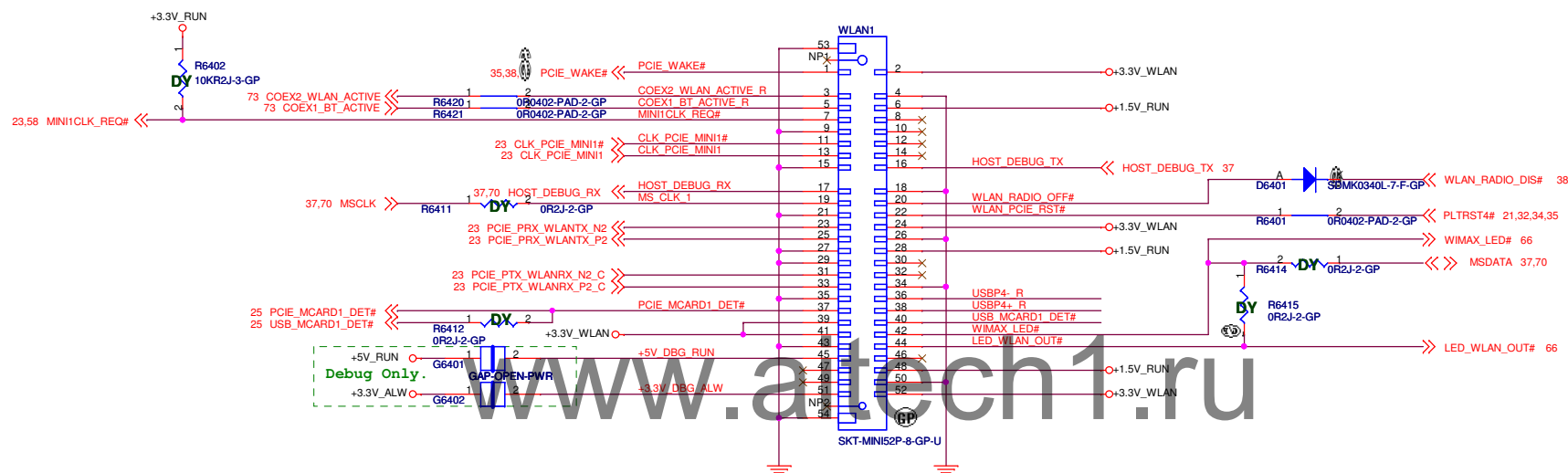
SSID = WLAN



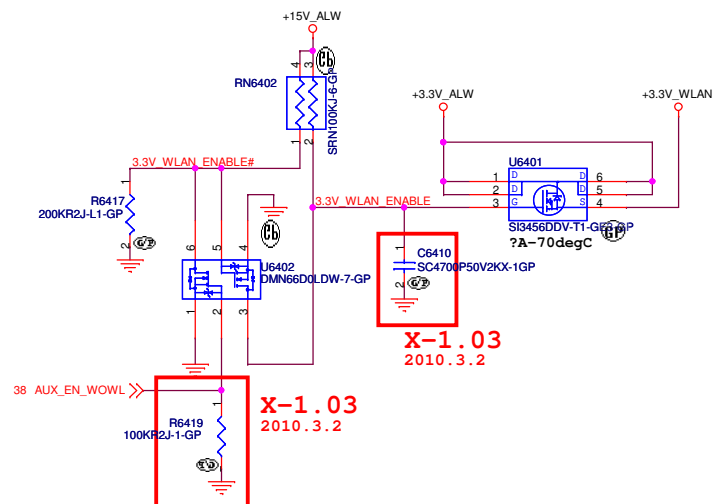
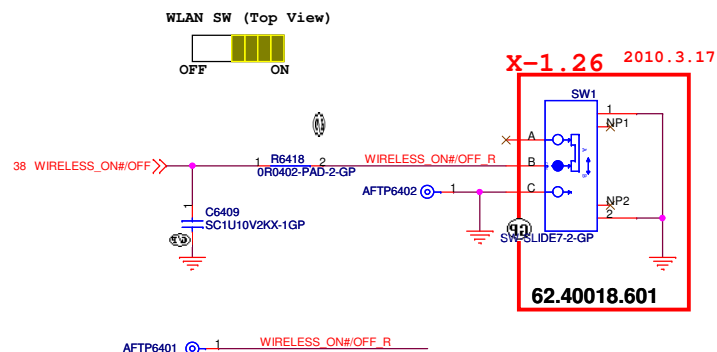
## DEBUG PINS

JMINI Pin	Debug Pin Name	EC Pin
16	HOST_DEBUG_TX	B44
17	HOST_DEBUG_RX	B46
19	8051_TX	B43
42	8051_RX	A40

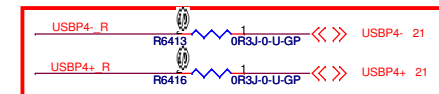
### MiniCard WLAN connector



## Wireless Switch



**x-1.19**      2010.3.10



Close WLAN1

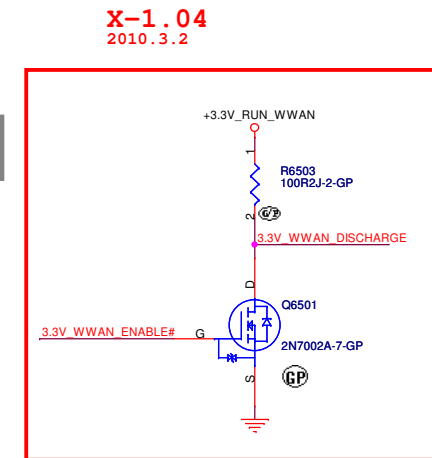
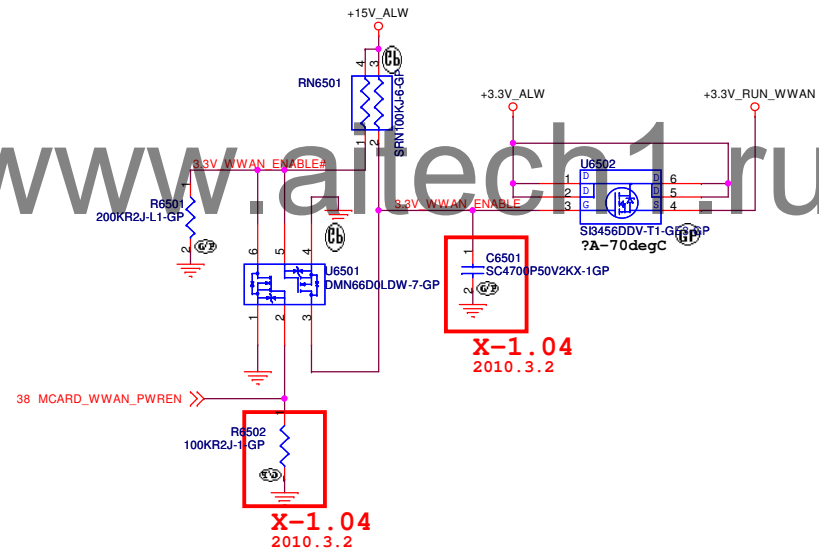
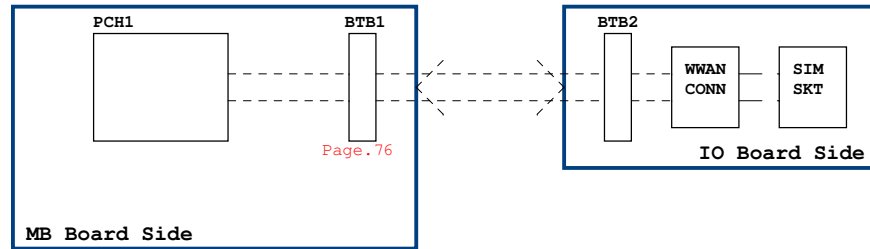
### <Core Design>

**DELL** **Wistron Corporation**  
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Taipei Hsien 221, Taiwan, R.O.C.

Title **WLAN / Serial Out Connector**

Size Custom	Document Number <b>Fonseca UMA</b>	Rev <b>X02</b>
Date: Thursday, March 18, 2010	Sheet 64 of 82	

**SSID = WWAN**

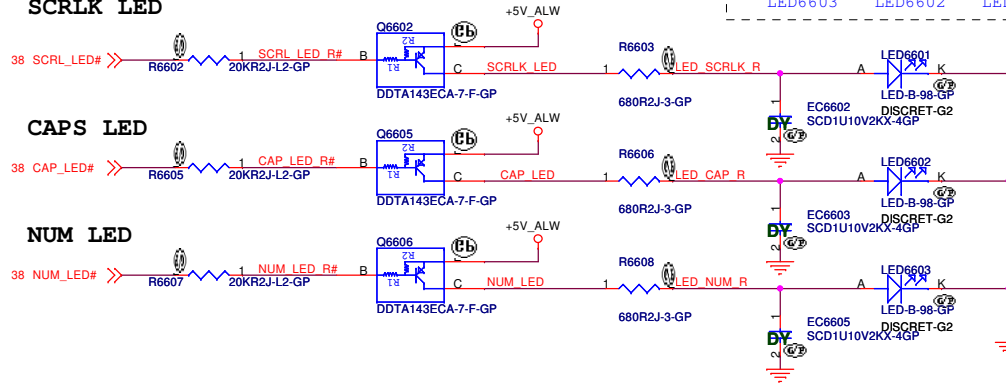


# SSID = User.interface

LED Location from left to right  
(MB, Top View)

NUM CAPS SCRLK  
LED6603 LED6602 LED6601

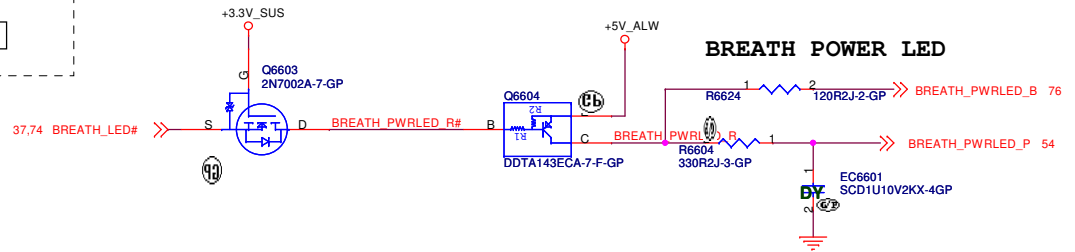
## SCRLK LED



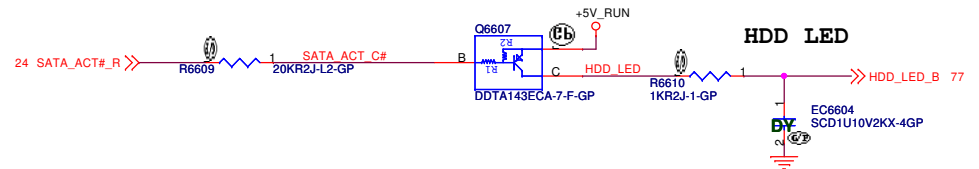
## CAPS LED

## NUM LED

## BREATH POWER LED



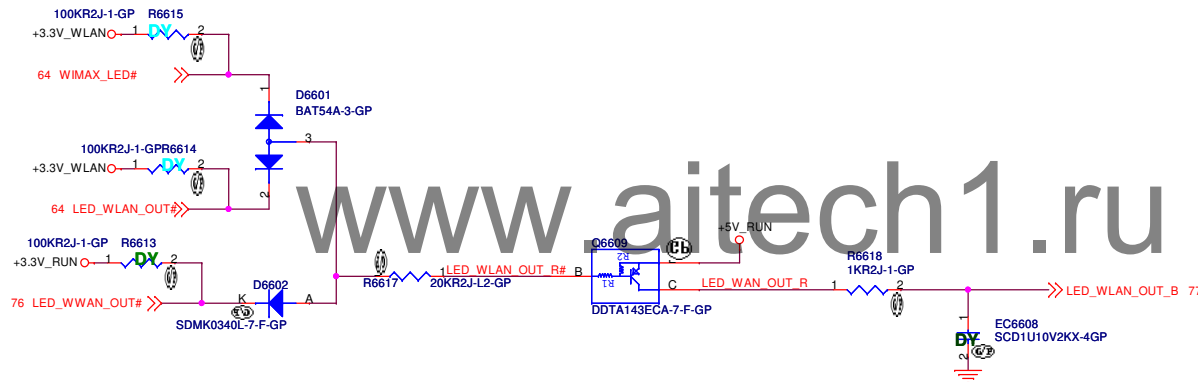
## HDD LED



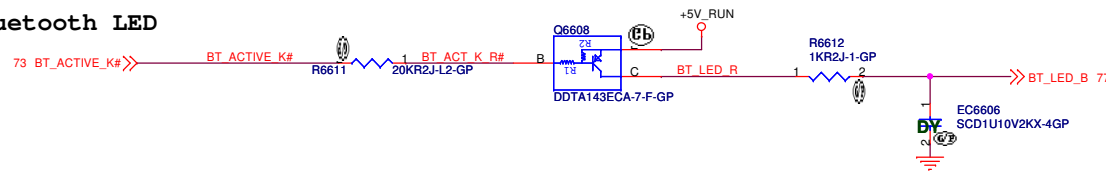
## WIMAX LED

## WLAN LED

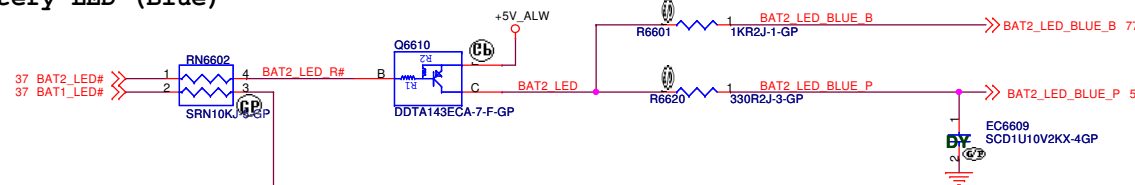
## WWAN LED



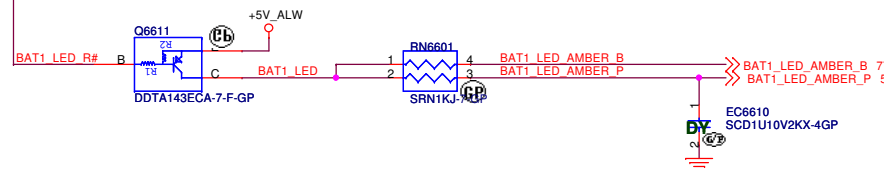
## Bluetooth LED



## Battery LED (Blue)



## Battery LED (Amber)



<Core Design>

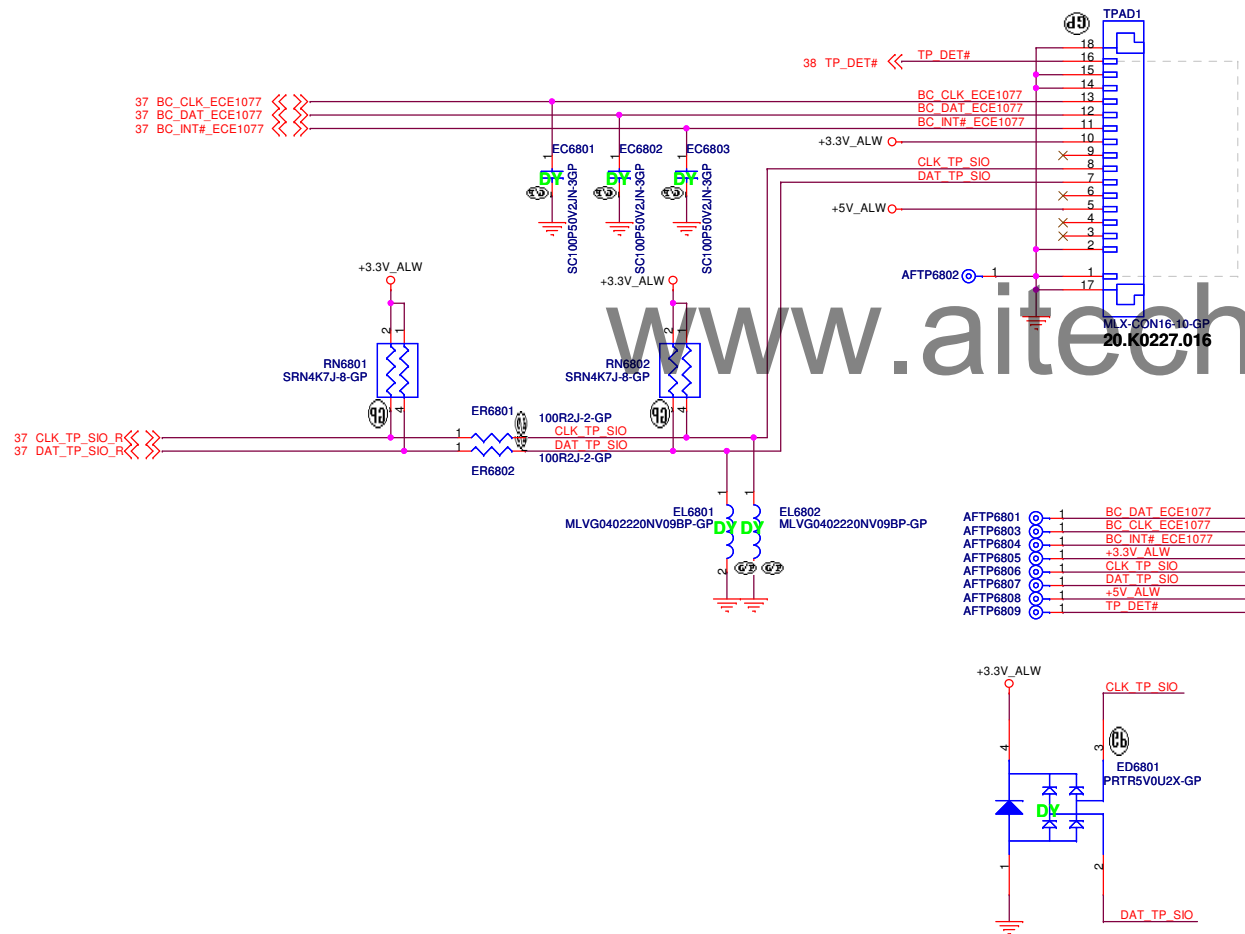
**DELL** Wistron Corporation  
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Title	LED	
Size	Document Number	Rev
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SSID = Touch.Pad

## TouchPad Connector



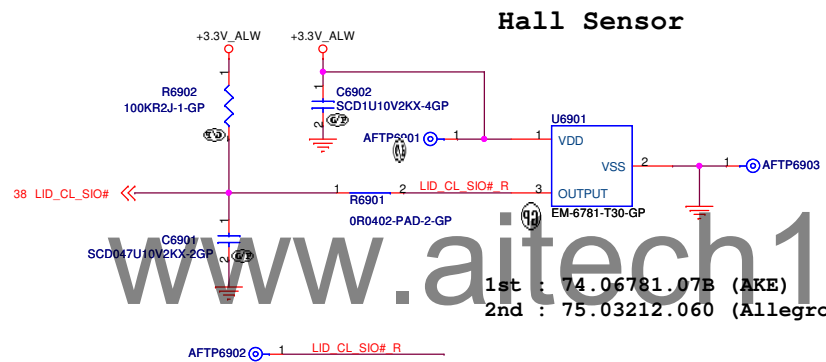
### Touch PAD Module Side

16	TP_DET#
15	GND
14	GND
13	BC_CLK (ECE1077)
12	BC_DAT (ECE1077)
11	BC_INT# (ECE1077)
10	3.3V_ALW
09	3.3V_RUN (Internal NC)
08	PS2_CLK
07	PS2_DATA
06	5V_RUN (Backlight, No Use)
05	5V_ALW (Chip change to use 3V, NC)
04	PWM (Backlight, No Use)
03	GND (Backlight, No Use)
02	GND
01	Diag_loop

<Core Design>



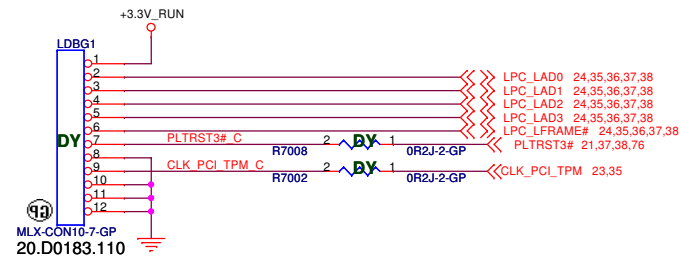
```
SSID = User.interface
```



1st : 74.06781.07B (AKE)  
2nd : 75.03212.060 (Allegro)

SSID = User.Interface

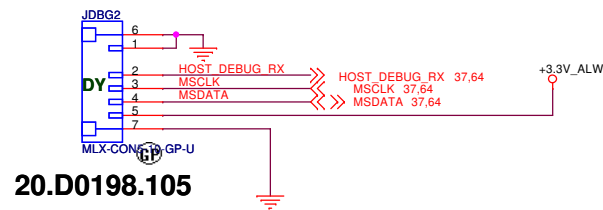
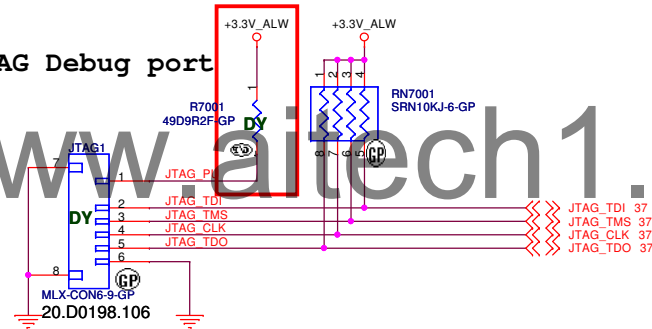
### LPC Debug port



LDBG1, need pop R7008, R7002

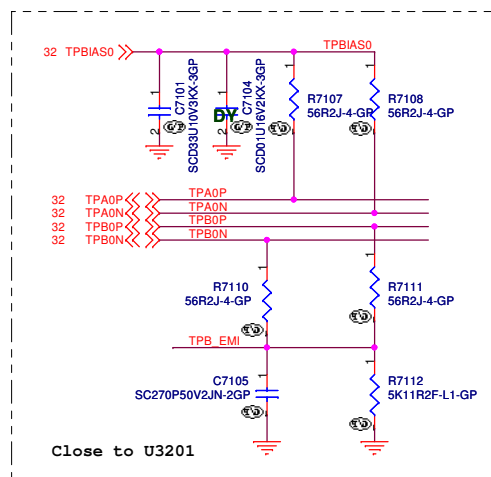
X-1.22 2010.3.10

### JTAG Debug port



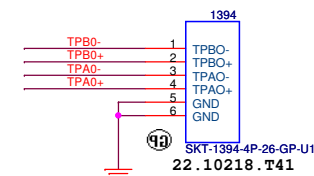
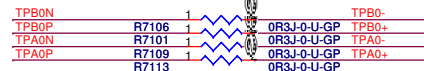
<Core Design>

SSID = 1394



Shield GND separately for pairs of  
TPA+ & TPA- and TPB+ & TPB-

X-1.10 2010.3.2



&lt;Core Design&gt;



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Title

### **1394 Connector / Flash Socket**

Size  
A

Document Number

**Fonseca UMA**Rev  
**X02**

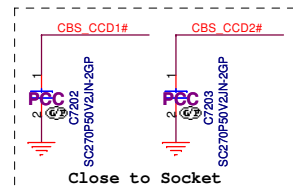
Date: Wednesday, March 17, 2010

Sheet 71 0

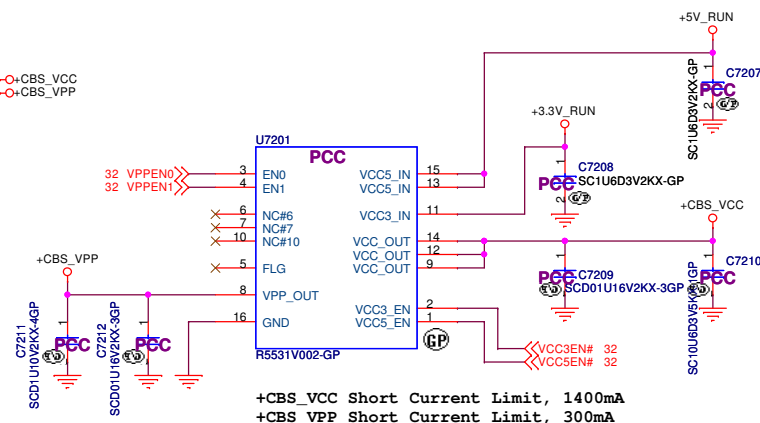
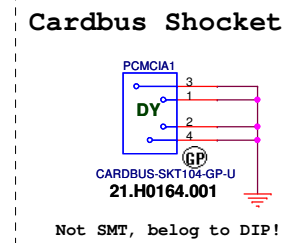
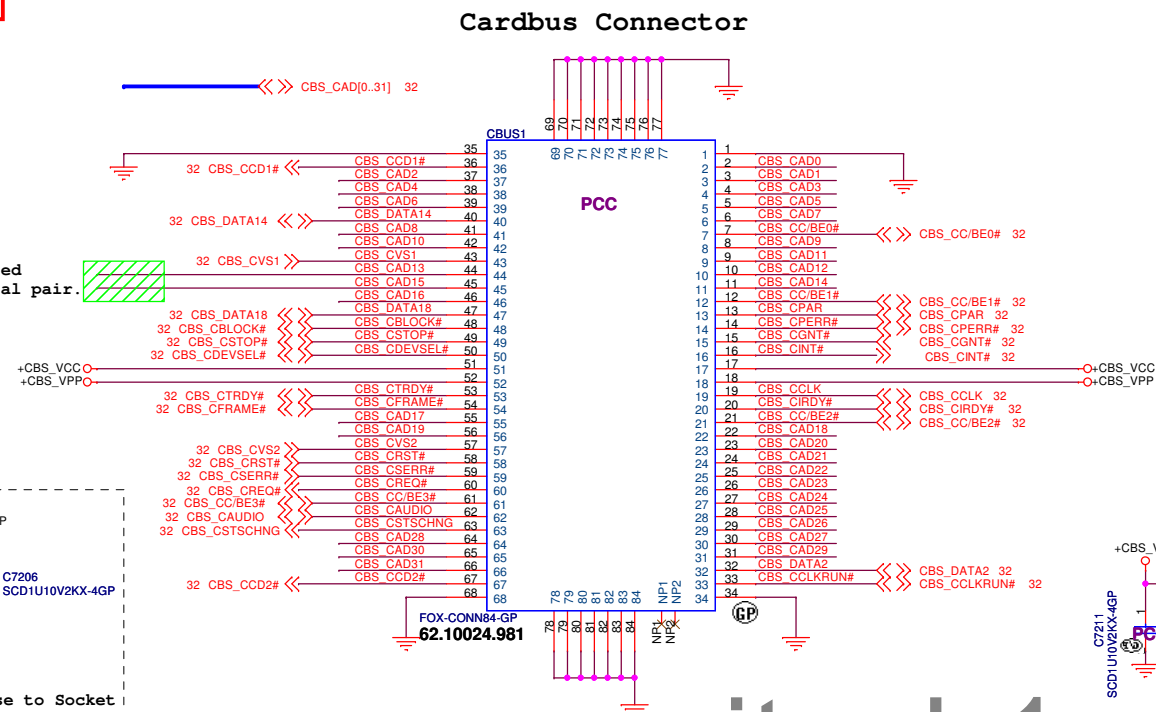
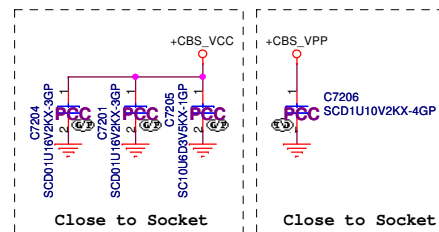
---

82

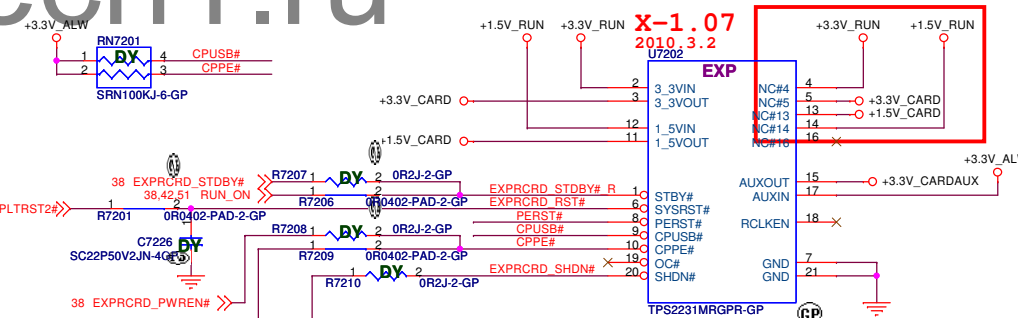
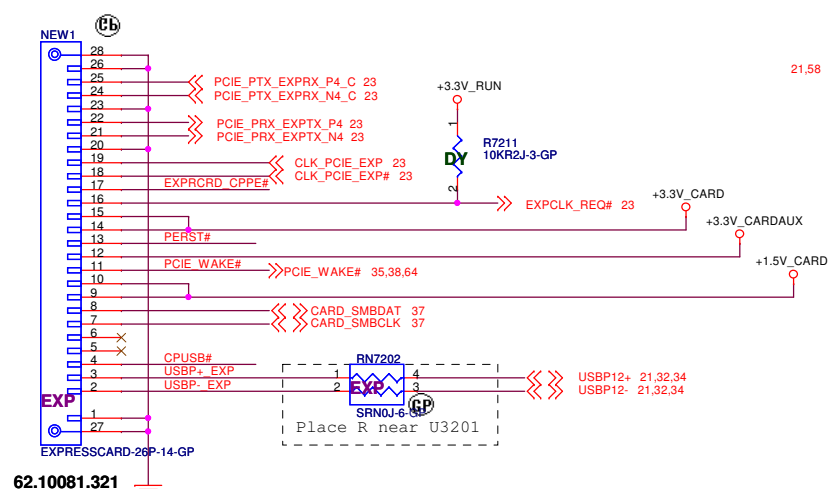
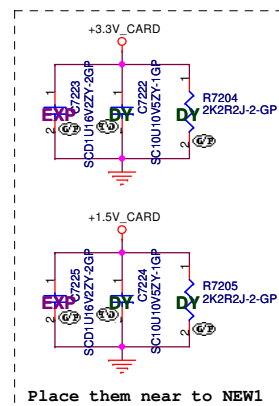
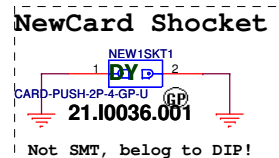
**SSID = CARDBUS**



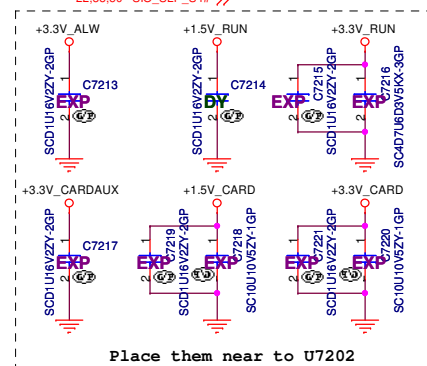
CBS\_CAD13, CBS\_CAD15 Can be used  
as Express Card USB differential pair.



```
SSID = ExpressCard
```



+1.5V\_CARD Max. 650mA, Average 500mA.  
+3.3V\_CARD Max. 1300mA, Average 1000mA  
+3.3V\_CARDAUX Max. 275mA



## <Core Design>



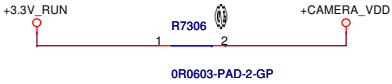
**Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title	<b>PCMCIA / ExpressCard</b>
-------	-----------------------------

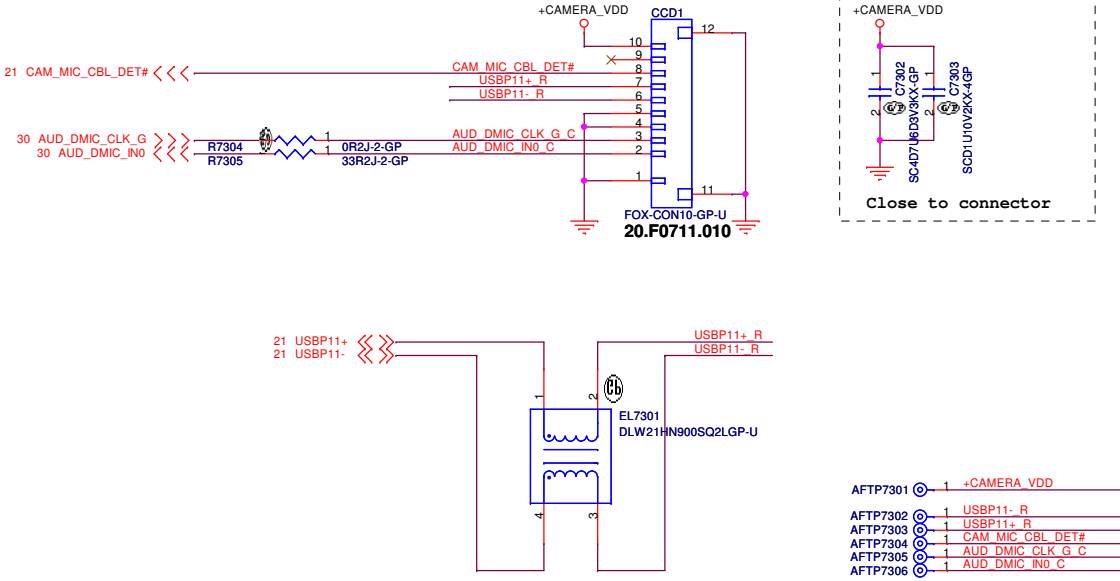
Size A3	Document Number <b>Fonseca UMA</b>	Rev X02
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SSID = User.interface

Camera Power CTRL



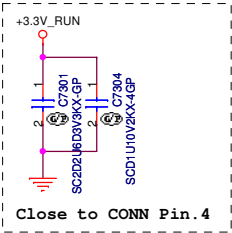
Camera Connector



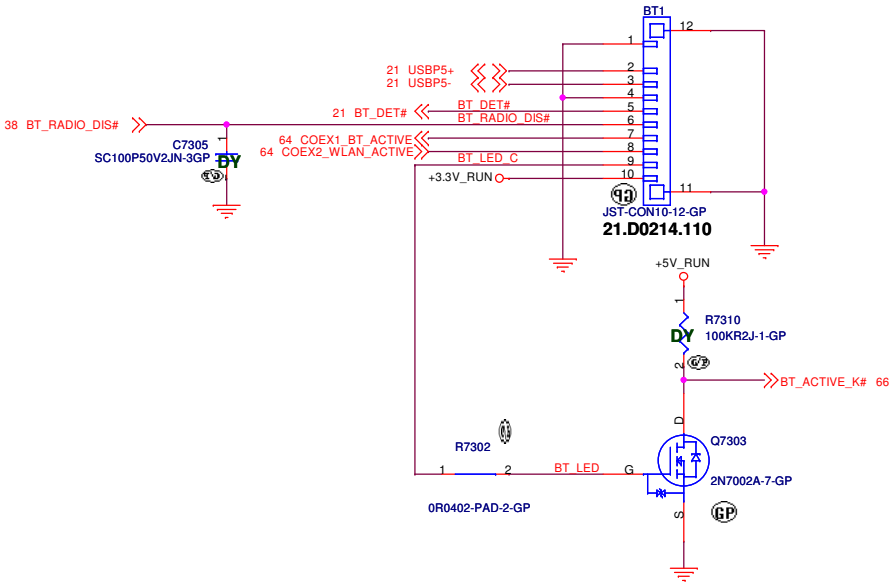
SSID = User.interface

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Bluetooth Connector



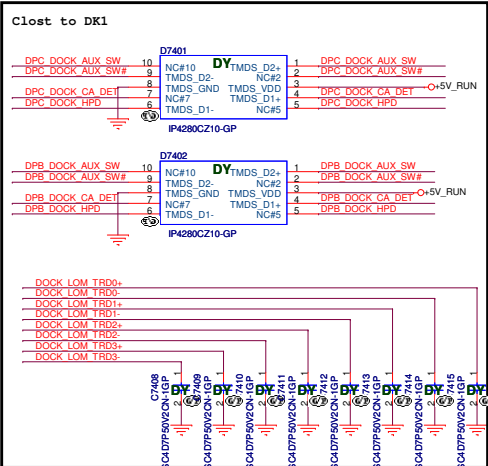
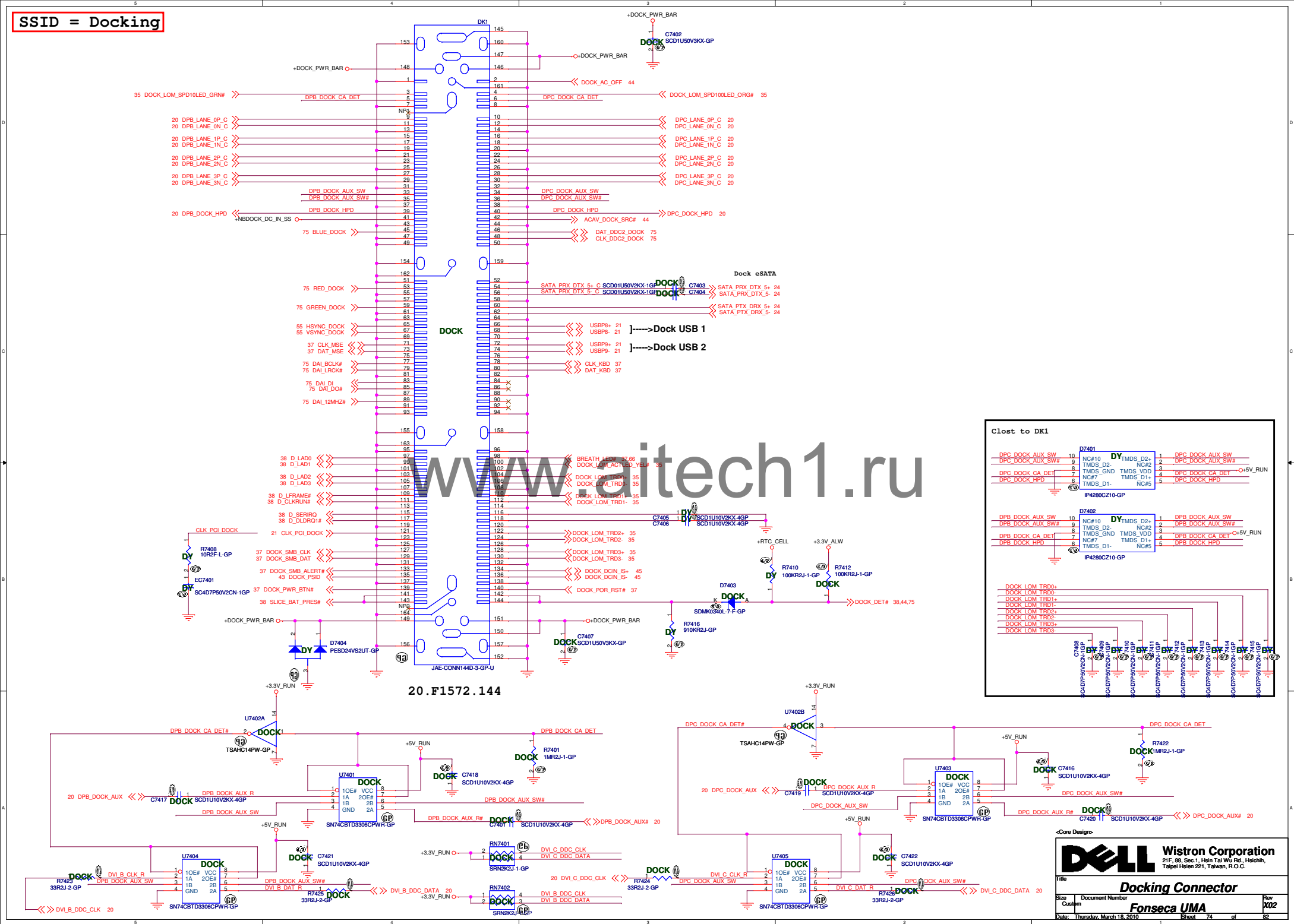
- AFTP7307 1 +3.3V\_RUN
- AFTP7308 1 COEX1\_BT\_ACTIVE
- AFTP7309 1 COEX2\_WLAN\_ACTIVE
- AFTP7310 1 USBP5+
- AFTP7311 1 BT\_RADIO\_DIS#
- AFTP7312 1 BT\_LED
- AFTP7313 1 BT\_DET#
- AFTP7314 1 BT\_DET#



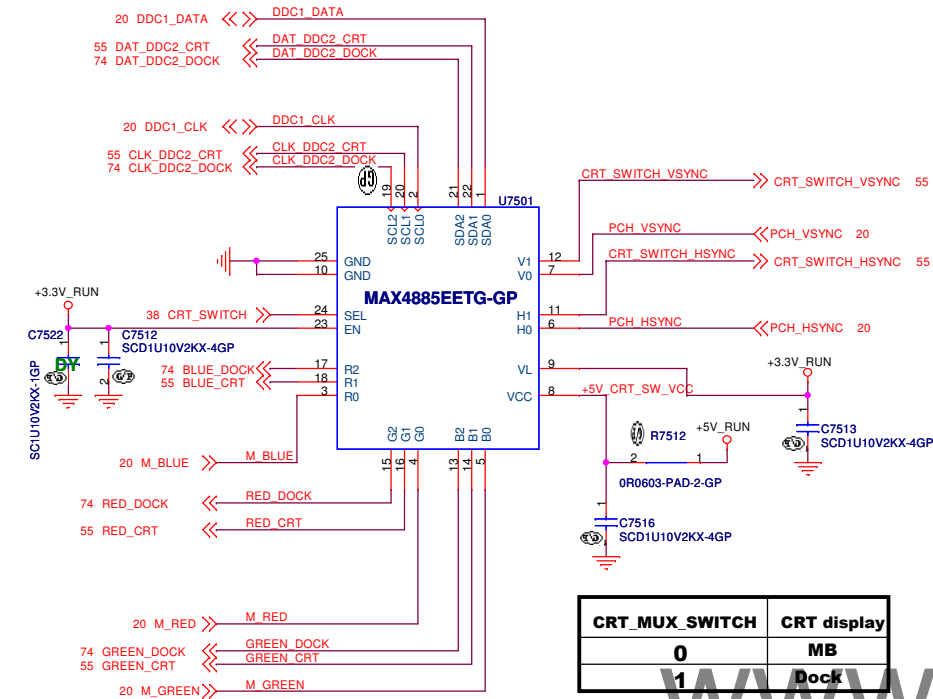
MB BT CONN

PIN	Define	PIN	Define
1	GND	1	GND
2	USBP5+_R	12	USB_DP
3	USBP5-_R	11	USB_DN
4	GND	10	GND
5	BT_DET#	2	MOD_DET
6	BT_RADIO_DIS#	7	RADIO_DIS
7	COEX1_BT_ACTIVE	3	COEX1_BT_ACTIVE
8	COEX2_WLAN_ACTIVE	8	COEX2_WLAN_ACT
9	BT_LED	6	LINK_IND
10	+3.3V_RUN	9	3.3V
11	NC		
12	NC		

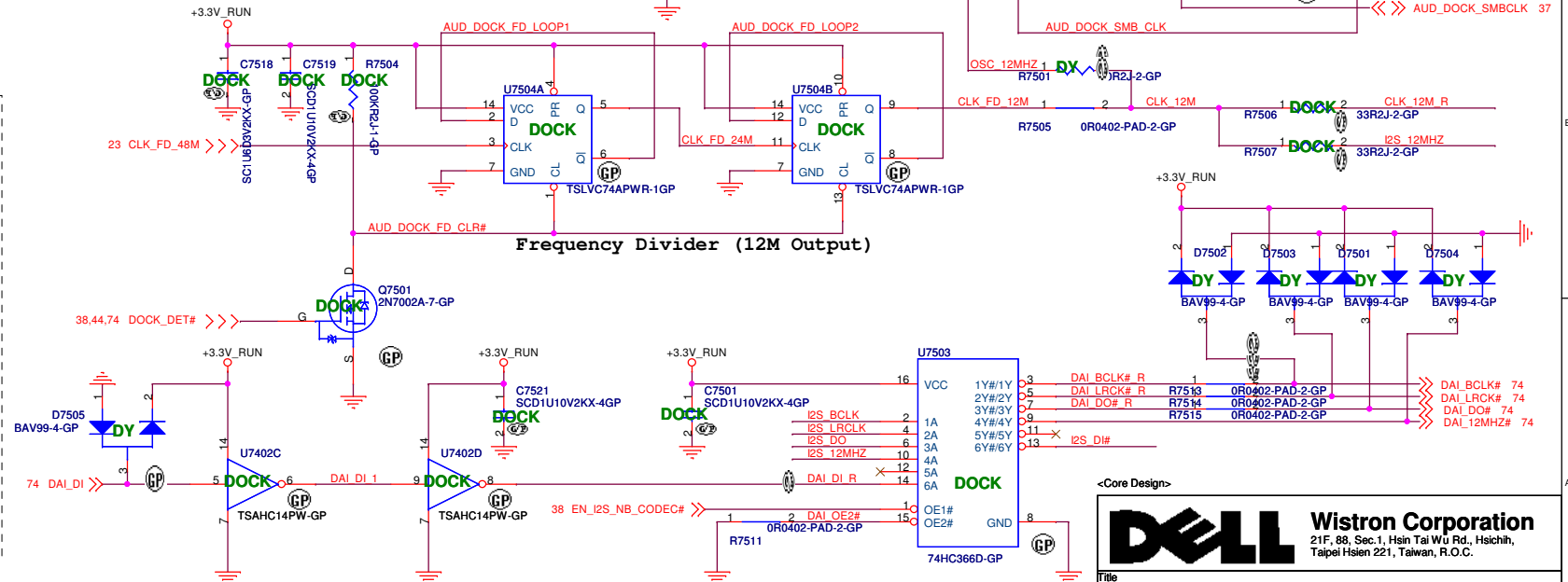
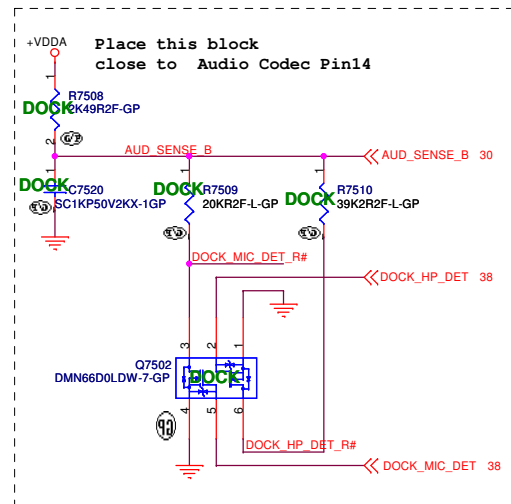
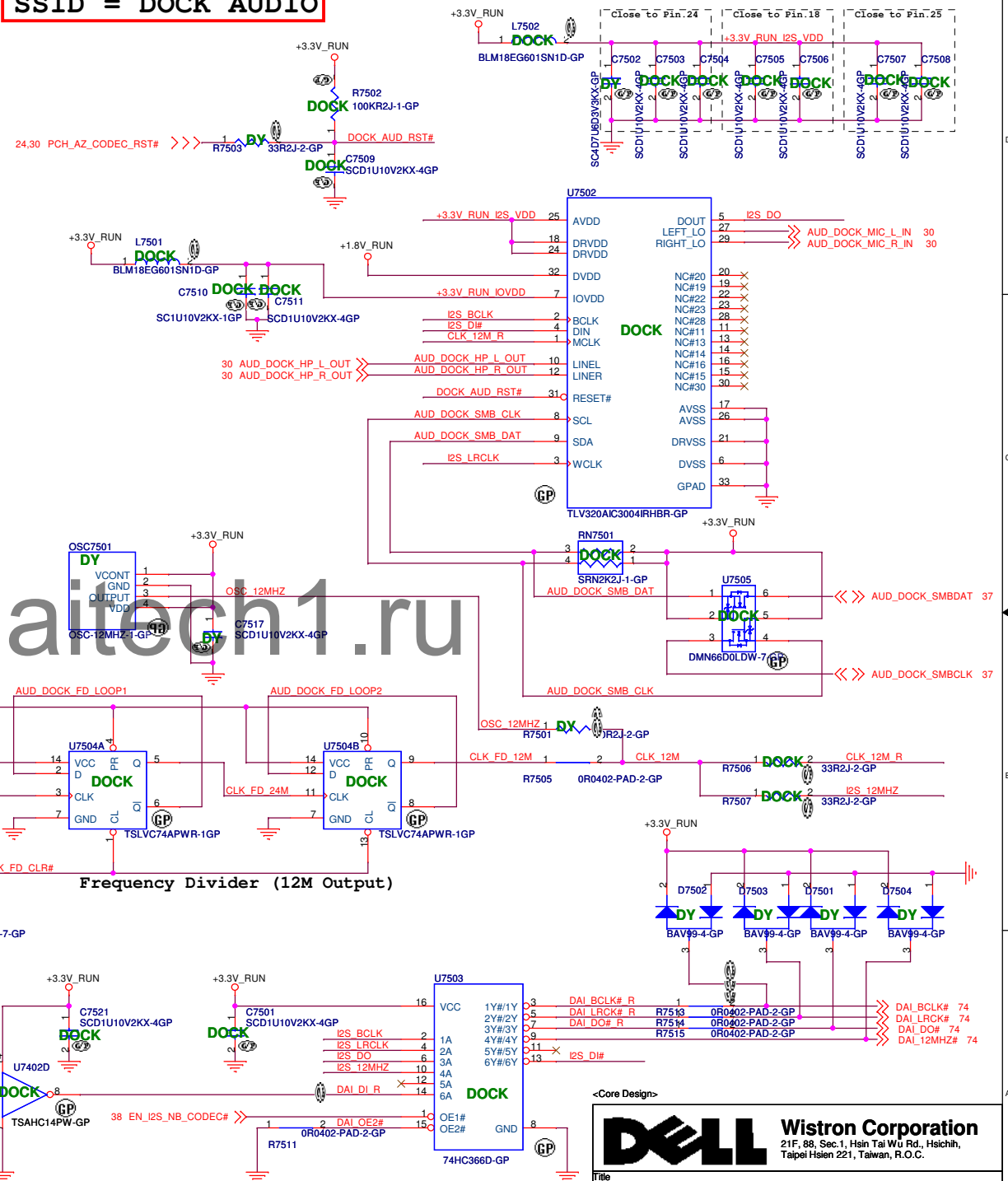
SSID = Docking



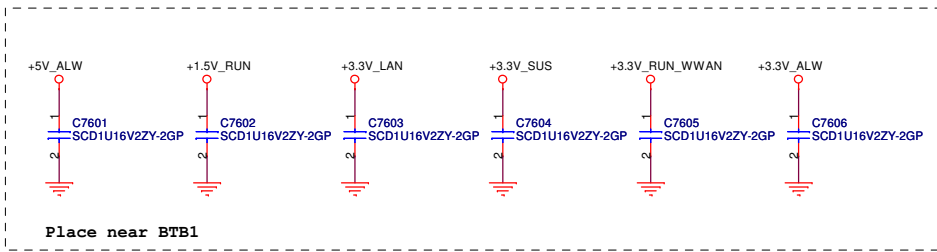
## SSID = DOCK CRT SWITCH



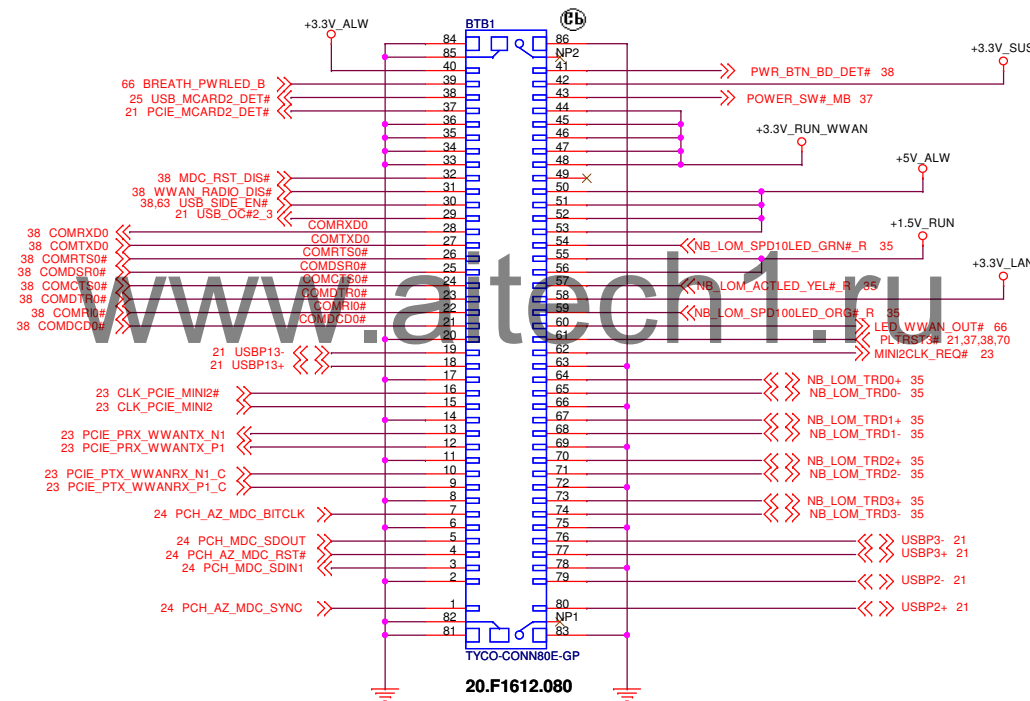
## SSID = DOCK AUDIO



# SSID = User.Interface



## IO Board Connector



<Core Design>

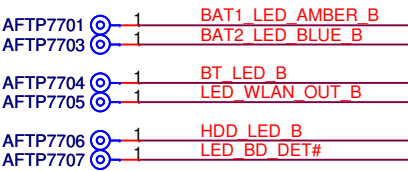
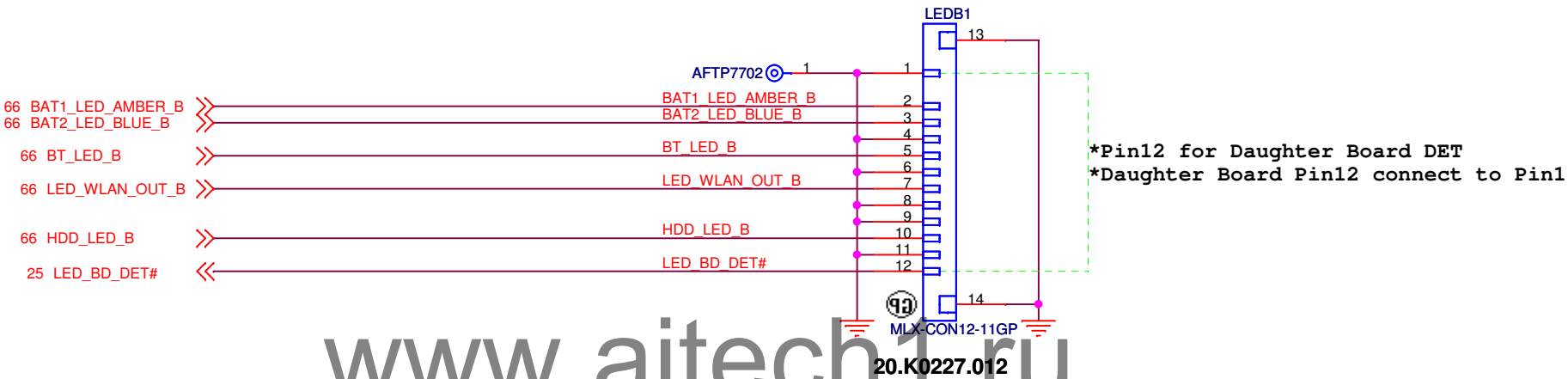


Title				
<b>IO Board CONN</b>				
Size A3	Document Number <b>Fonseca UMA</b>			Rev <b>X02</b>
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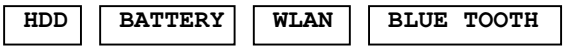


SSID = User.interface


LED BD Connector



LED Location from left to right



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Title

**LED Board Connector**

Size  
A4

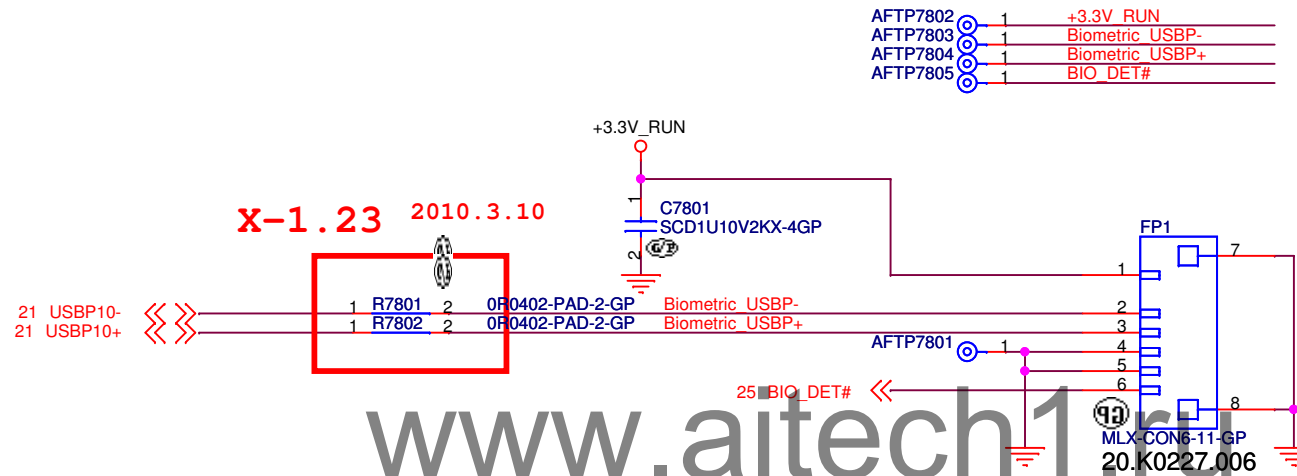
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**Fonseca UMA**

Rev  
**X02**

Date: Thursday, March 18, 2010

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SSID = User.Interface



Biometric Connector

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Title

**Finger Printer Board CONN**

Size  
A4

Document Number

**Fonseca UMA**

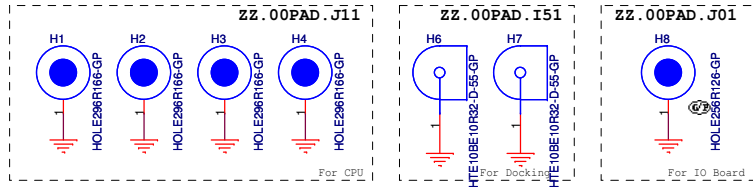
Rev  
**X02**

Date: Thursday, March 18, 2010

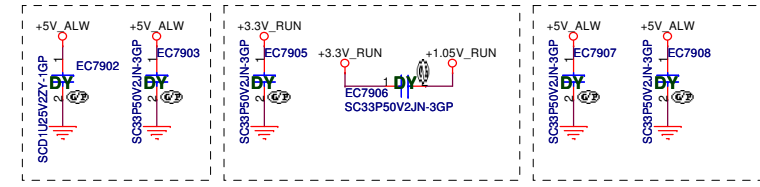
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# SSID = Mechanical

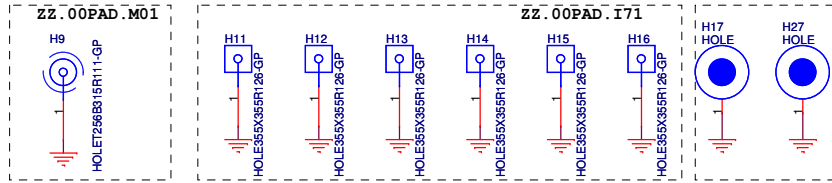
Hole



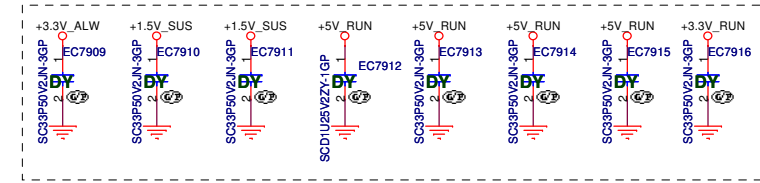
RF Cap.



Hole

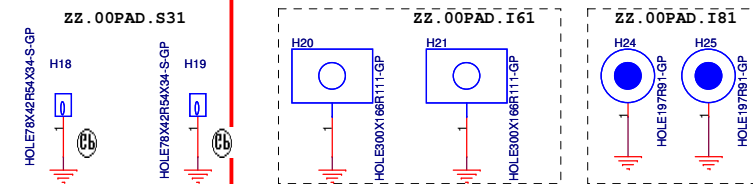


RF Cap.

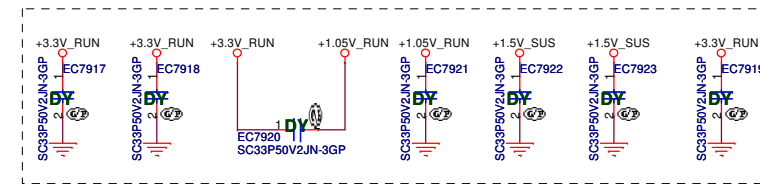


Hole

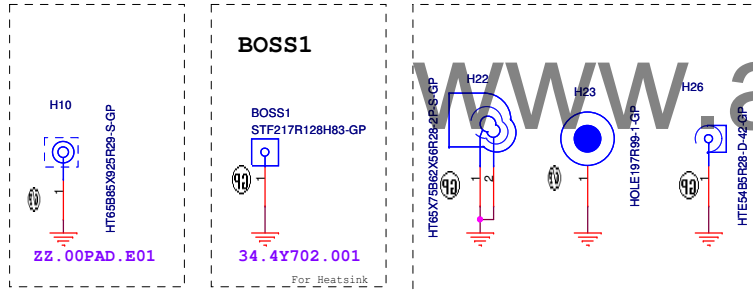
X-1.27  
2010.3.17



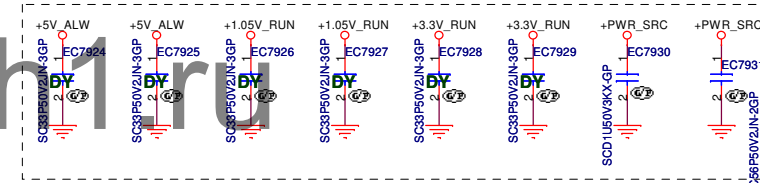
RF Cap.



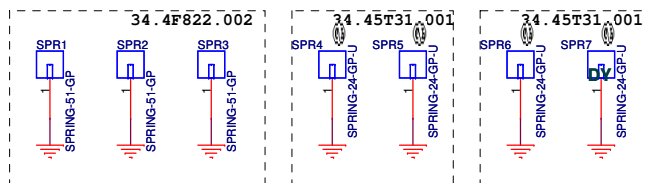
Hole



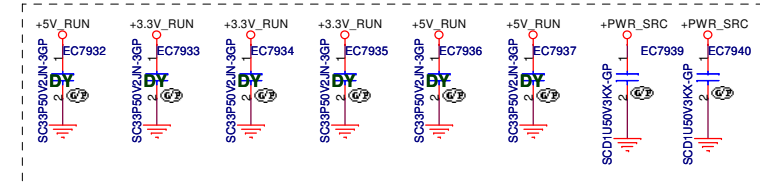
RF Cap.



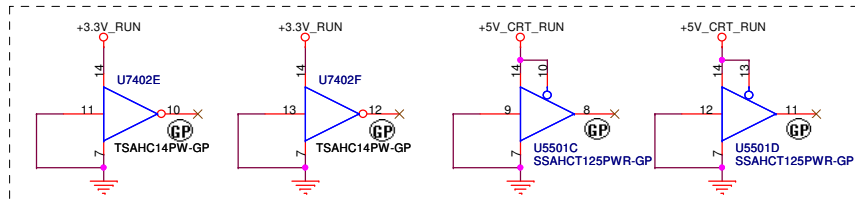
Spring



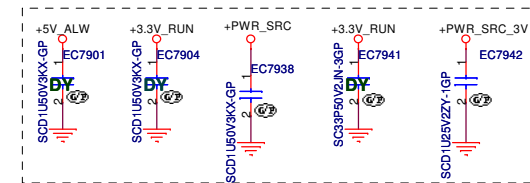
RF Cap.



Unused Parts



EMI Cap.



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Title  
**Unused Parts / EMI RF Cap.**

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DATE	NO	PAGE	ACTION	reference	Issue Description	OWNER
20100302	X-1.01	47	change	PTC4701 --->DY PTC4702 --->POP	change cap place location for factory request.	EE
	X-1.02	58	DY	XDP1,XDP2,C5802,C5803,R5803,R5804,R5806,R5808	change to DY part number for layout used.	EE
	X-1.03	64	STUFF	C6410,R6419	C6410 --> soft start R6419 --> quick discharge	EE
	X-1.04	65	STUFF	C6501,R6502,R6503,Q6501	C6501 --> soft start R6502,R6503,Q6501 --> quick discharge	EE
	X-1.05	42	Change	C4208	change to 470P for soft start used	EE
	X-1.06	51	ADD	PC5108	reserve location	POWER-EE
	X-1.07	72	ADD	U7202	add pin4,5,13,14 for second source	EE
	X-1.08	37	Change	R3703	change board ID to -1	EE
	X-1.09	37, 54	ADD	R3741,Q5404,R5428,R5429,C5412,U5402,C5410,C5411	add power switch to control lcd power	EE
	X-1.10	71	remove	L7504,L7101	remove co-layout part for PSE request	EMC
20100310	X-1.11	54	change	R5415	change part number to 63.10133.15L	EE
	X-1.12	58	change	TP5801~TP5815	change test pad to DY part for layout	EE
	X-1.13	7	remove	RN701,RN703,RN704,RN705	remove 0 ohm part for layout	EE
	X-1.14	23	change	RN2312,RN2313	change RN2312 ,RN2313 to short pad for layout	EE
	X-1.15	23	remove	RN2307,RN2308,RN2301	remove 0 ohm part for layout	EE
	X-1.16	25	remove	RN2501	remove 0 ohm part for layout	EE
	X-1.17	32	change	RN3201	change RN3210 to short pad for layout	EE
	X-1.18	40	STUFF	C4002		EE
	X-1.19	64	remove	EL6401	remove EL6401 for PSE request because it co-layout with resister.	PSE
	X-1.20	55	ADD	AFTP5501	add test pad for I/O test used	factory
	X-1.21	67	STUFF	C6704,C6705		EE
	X-1.22	70	DY	R7001	not use debug port	EE
	X-1.23	78	change	remove EL7801 change R7801,R7802 to short pad	remove EL7801 for PSE request because it co-layout with resister.	PSE
20100317	X-1.24	67	change	SC1 SC1SKT1	change connector type	ME
	X-1.25	63	remove	EL6301 EL6302	remove co-layout 0 ohm pad	PSE
	X-1.26	64	change	SW1	change connector type	PSE
	X-1.27	79	change	H18 H19	change hole type	ME
20100318	X-1.28	9	DY	R913 Q901 C901 R903		EE
	X-1.29	67	ADD	C6706		EE
20100319	X-1.30	67	change	C6704 C6705 R6705	change resister and capacitance value	EE

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Title			
<b>Change List (1/1)</b>			
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